Frame Design for Differential Packet-Level Index Modulation implemented by LoRaWAN

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***Abstract*—LoRaWAN is focused as one of standards for LPWA (Low Power Wide Area) that is employed in IoT (Internet of Things) system. In order to realize a packet-level index modulation (PLIM), this paper implements the sensor nodes with LoRaWAN. In this paper, a differential PLIM (DPLIM) which is based on PLIM without a time frame synchronization is studied. The use of DPLIM implemented in LoRaWAN requires the design of a new time frame to transmit at any given time. The new time frame design is based on the specification of LoRaWAN that the sensor node has to open two receive windows after transmits a packet. This paper uses the implemented wireless sensor node and confirms the performance of DPLIM that is better than that of conventional PLIM.**

***Index Terms*—Low Power Wide Area, LoRaWAN, Packet-Level Index Modulation, Differential Packet-Level Index Modulation**

I. Introduction

In recent years, the development of the Internet of Things (IoT) has raised expectations for Low Power Wide Area (LPWA). While LPWA is expected to be applied to systems that originally have no problem with low communication rates, a slight increase in communication rate increases the versatility of LPWA. However, LPWA cannot increase the number of transmission bits by increasing the transmission period because the transmission time ratio (Duty Cycle) has to be less than 1% according to radio laws and regulations [1].

Packet-Level Index Modulation (PLIM) is proposed for LPWA systems as a method which can add a few data bits to indexes of time slot and frequency [2]. In the PLIM, the sensor node and the gateway have to share the information on the beginning of the time frame for detecting the time slot index at which a received packet was transmitted. In addition, the PLIM needs to perform time synchronization regularly and repeatedly, because the sensor nodes of IoT system are equipped with low accurate oscillators. Therefore, a differential PLIM (DPLIM) which is based on the PLIM is proposed [3]. The DPLIM can convey PLIM symbols without time synchronizations.

In DPLIM, PLIM symbols are mapped to a difference between transmission times of consecutive packets. A receiver can transfer the difference between the times of the received consecutive packets into symbols which is added in the same way as the PLIM. The DPLIM does not need to pay costs for time synchronization due to the received time of the one previous packet as the time reference. In this paper, a wireless sensor node that performs DPLIM transmission under microcontroller control was fabricated. The LoRaWAN module is mounted on that wireless sensor node. This paper evaluates the time index demodulation errors with conventional PLIM method and proposed DPLIM method by the actual implemented sensor node.

II. Differential Packet-Level Index Modulation (DPLIM)

At first, this section briefly introduces a differential packet-level index modulation scheme. The sensor nod with DPLIM uses the difference between the transmission time of one previous $i-1$-th packet and the transmission time of the i-th packet to assign a symbol to the index of a time slot, and then can transmit additional bits. This section describes the DPLIM method used to transmit packets from an IoT node with node number m to a gateway as a receiver. The header of a packet contains the node number and packet number, and a packet transmission is defined as being transmitted only once in a frame which is a fixed time interval. Frames are slotted, and the slot length is longer than the packet length. There are no retransmissions, and the node determines the time slot index at which to transmit a packet for each frame and performs the packet transmission. The DPLIM scheme can also add data to the frequency index, but this paper only describes the time slot index, which is affected by clock drift.

A. Determination of transmission time in DPLIM

When the i-th packet is generated at the node which is an IoT node, the index q_i of the time slot to transmit the packet is determined from the data D_i which is conveyed by DPLIM. The determination formula is expressed as follows,

$$q_i = (D_i + q_{i-1}) \bmod Q, \tag{1}$$

where Q is the number of indices in DPLIM. A transmit node sends the i-th packet at the time corresponding to q_i. Since

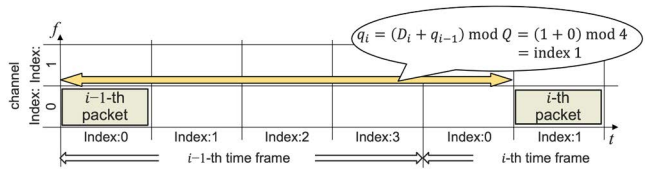

Fig. 1. Data mapping in DPLIM

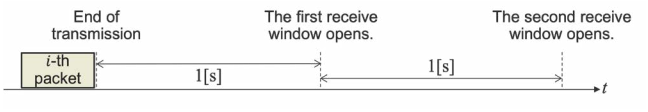

Fig. 2. Receive windows in LoRaWAN class A [4]

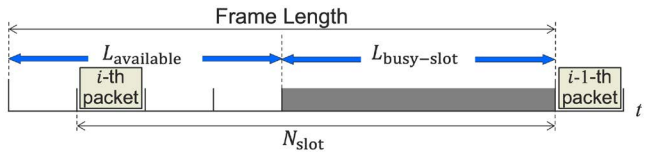

Fig. 3. Time frame composition

the first packet has no previous packet, the node arbitrarily determines the transmission index and sends the first packet at the time corresponding to that index, as shown in Figure 1.

B. Detection of Time Slot Index in DPLIM

After receiving a packet, the receiver which is a gateway demodulates the packet number i and node number m from the header of the packet. The gateway calculates the difference between the reception time t_i of the i-th packet sent from the node m and the reception time t_{i-1} of the one previous packet that is transmitted from the node m and the packet number is $i-1$. Then the data D_i sent by DPLIM is directly demodulated from the difference using the following formula,

$$\overline{D_i} = \left\lfloor \frac{t_i - t_{i-1}}{T_{\mathrm{S}}} + 0.5 \right\rfloor \bmod Q, \tag{2}$$

where T_{S} is the slot length. The difference between received times of the consecutive packets is treated in units of slots rather than seconds by dividing the received time difference by the slot length and rounding it to the nearest whole number using the floor function. The remainder of the number of slots between received packet with previous packet number and the received packet divided by the number of index, Q, allows demodulation of the data symbols (time slot indices) transmitted by DPLIM. Here, when the time between received packets is treated in units of slots, the number of slots between received packets, N_{slot}, is defined as follows,

$$N_{\text{slot}} = \left\lfloor \frac{t_i - t_{i-1}}{T_{\mathrm{S}}} + 0.5 \right\rfloor. \tag{3}$$

Using N_{slot}, the expression (2) can be restated as follows,

$$\overline{D_i} = N_{\text{slot}} \bmod Q. \tag{4}$$

C. Features of DPLIM

In DPLIM, the index to which a data symbol is assigned is estimated from the reception time between consecutive packets sent by a node m, as in the PLIM scheme. Thus this eliminates the cost of periodic frame synchronization that has been necessary with the simple PLIM scheme. Since it is difficult to know the absolute time for nodes not equipped with GPS, etc, information about the start time of a frame must be shared between the transmitter node and receiver (gateway) to synchronize frames. The reason why GPS cannot be installed in IoT wireless nodes is that it is difficult to install in the vast number of wireless nodes used for IoT, due to its low price and the need to suppress power consumption since battery operation is a prerequisite.

On the other hand, the DPLIM system requires the reception time of one previous packet to demodulate the index. Thus when the previous packet cannot be demodulated or one packet loss occurs, demodulation of the index of DPLIM becomes impossible. Even a single packet loss will result in the loss of two symbols worth of information because it prevents the demodulation of the index of the lost packet and the index of the next received packet. Therefore, the impact is greater in an environment where packet loss occurs frequently and intermittently. which has a significant impact in environments with frequent packet loss.

III. Time Frame Design for DPLIM Scheme Implemented on LoRaWAN

When the index of a time slot is demodulated, the performance of DPLIM is affected only by the accumulated clock drift between consecutive packets, thus mitigating the effect of index demodulation error due to clock drift. In this paper, DPLIM is implemented by using LoRaWAN, a type of LPWA, because it is easy to implement and can be used without a license. Therefore, the frame design for DPLIM according to the LoRaWAN specifications is necessary for the actual implementation.

This paper implements the sensor node by employing LoRaWAN Class A [4]. In LoRAWAN class A, communications are initiated by sensor nodes. The sensor node must open two short receive windows for receiving a packet transmitted from a gateway after transmitting its own packet as shown in Figure 2. The timings of the opening of the receive windows shown in Figure 2 are the default parameters. These receive windows are determined by LoRaWAN specifications [5], [6]. In practice, the receive windows of the sensor node are opened one second and two seconds after the packet is sent, respectively. Therefore, to take reception processing into account, a period consisting of time for a reception processing and time for preparing to send the next packet was set up after the PLIM slot term, $L_{\text{available}}$, in which the packet is transmitted.

As shown in Figure 3, this paper reconfigures the frame with $L_{\text{available}}$, the period during which packets can be sent, and

TABLE I
PARAMETERS FOR LORAWAN

Center frequency	CF	923.4 MHz
Channel bandwidth	BW	125 kHz
The number of symbols per packet	SY	45.25 symbols
Spreading Factor	SF	8
Time on Air	ToA	93 ms

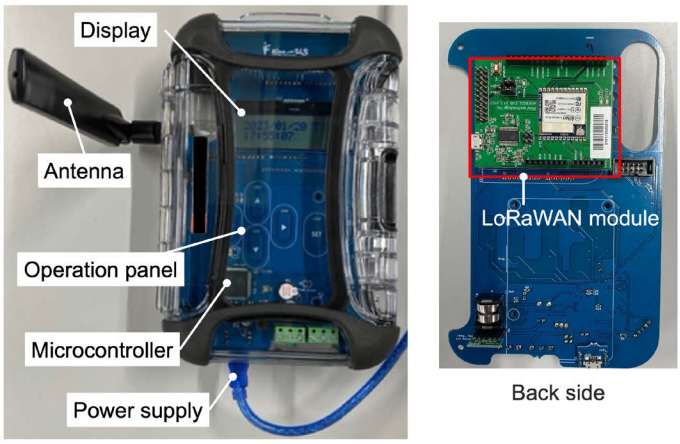

Fig. 4. Implemented sensor node

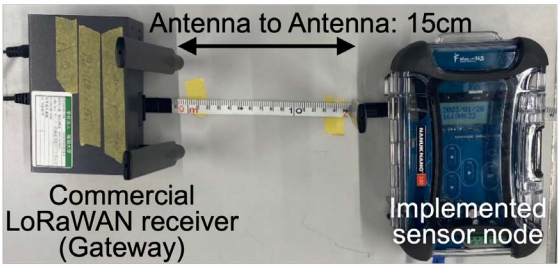

Fig. 5. Experimental system

TABLE II
EQUIPMENTS FOR EXPERIMENTS

LoRaWAN gateway	TLG2901B-J01S (Kiwi Technology Inc.)
LoRaWAN module	ADB922S (Kiwi Technology Inc.)
Microcontroller	PSoC5LP series CY8C5467AXI-LP108 (Infineon Technologies AG) CPU frequency : 64.5 MHz
Distance between sensor node and gateway	15 cm

L_{busy}, the period during which reception and other processing are performed in consideration of LoRaWAN specifications.

Here, in order to treat in slot units, $N_{\text{busy-slot}}$ is defined as the processing time, L_{busy}, divided by slot length and the remainder rounded up. With $N_{\text{busy-slot}}$, Eq. 4 is rewritten as follows, taking into account the processing times,

$$\widetilde{D_i} = \{(N_{\text{slot}} - N_{\text{busy-slot}}) \bmod N_{\text{F-slot}}\} \bmod Q. \quad (5)$$

$N_{\text{F-slot}}$ is the value of the frame length divided by the slot length. In Eq. 5, the surplus of the number of slots, $N_{\text{F-slot}}$, that make up the time frame is taken, so that the system can handle the case where there is no transmission in a frame interval for some reason. After that, index demodulation can be performed in this frame design by deriving the remainder by the index number Q as before.

IV. PERFORMANCE EVALUATIONS

A. Settings for evaluation

The parameters used in this experiment for LoRaWAN are listed in Table I, and the Time on Air value is calculated by the following equation [7],

$$ToA = \frac{2^{SF}}{BW} \times SY. \quad (6)$$

Based on the derived ToA, the slot length is set to 100 ms in our experiments so that the slot length is longer than the packet length.

Figure 4 is our implemented sensor node which is equipped with a PSoC5LP series microcontroller. The wireless part of our sensor node is controlled by the microcontroller. In our experiments, ADB922S manufactured by Kiwi Technology Inc. is used as the LoRaWAN module for the sensor node as shown in Table II. This paper uses LoRaWAN Class A for the packet communications.

Fig. 5 shows the experimental system in this paper. The implemented sensor node is connected to a commercial LoRaWAN gateway 15 cm apart. In our experiments are conducted as a one-to-one communication between the implemented sensor node and a commercial LoRaWAN gateway.

B. Index demodulation error rate using the implemented sensor node

$L_{\text{available}}$ and L_{busy} of which a frame for implementation consists, in our experiments, are 4 slots (0.4 seconds) which equals the number of time slot indexes and 30 slots (3.0 seconds) for receive processing and next packet generation processing, respectively. Table III shows the parameters for the experimental system. In this paper, PLIM and DPLIM were implemented in the same wireless sensor node and experiments using PLIM and DPLIM were conducted for each. In the experiments, 500 PLIM symbols were randomly generated, the time slot index of the packet was determined according to each method, and the index was used to transmit the packet. In PLIM, the first packet is transmitted with index 0 and is used for frame synchronization. On the other hand, in DPLIM, the first packet is transmitted at certain index because it cannot use for PILM symbol transmission. Therefore, in our experiments, the number of transmit packets is 501 which is equal to the sum of the number of transmit PLIM symbols and one.

Figure 6 shows index demodulation error rate when using the implemented sensor node. The index demodulation error rate is derived for every five frames. From this figure, it is confirmed that the conventional PLIM method increases

TABLE III
PARAMETERS FOR EXPERIMENTS

The number of transmit packets	501
Slot length ($> ToA$)	100 ms
The number of bits per PLIM symbol	2 slots ($= \log_2 Q$)
The number of time slot indexes, Q	4 slots
The number of time slot indexes per time frame	30 slots
Length of time frames	34 slots

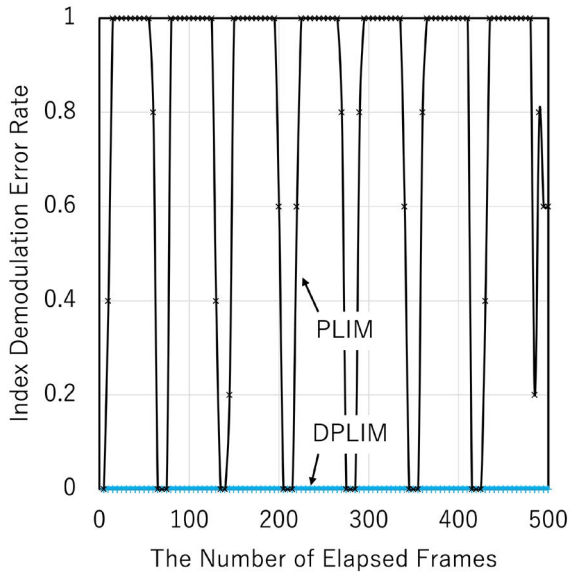

Fig. 6. Index demodulation error performance

periodic index demodulation errors caused by the clock drift with elapsed time. In addition, the index demodulation error in PLIM rapidly occurs after seven frames are passed from the time synchronization and that performance is repeated at a series of about 70 frames. From this result of PLIM, the PLIM in this system needs to perform a time synchronization per every seven frames. Periodic time-synchronized packets degrade the data transmission rate, and therefore the conventional PLIM is highly susceptible to clock drift. On the other hand, this experiment shows that the effect of clock drift on DPLIM is suppressed because the index demodulation error is 0 over the experiment time.

Figure 7 shows the probability of occurrence against the number of error-free frames from the next frame after synchronization in PLIM when 25 trials were performed. The value of the clock drift is constantly changing and is not constant and also occurs according to a normal distribution with respect to the mean value during short time periods. Therefore, when the accumulated clock drift happens to cancel out, the number of error-free frames increases. In addition, when the clock drift values are sufficiently accumulated, there is both a possibility of error and no error, depending on the timing of the index at which the packet is transmitted, even within the same frame. That is, if a packet is sent at an index with a late transmission

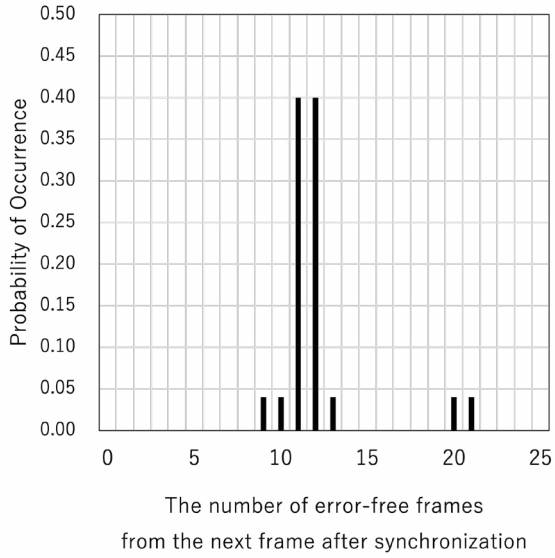

Fig. 7. Probability of occurrence against the number of error-free frames from the next frame after synchronization in PLIM (25 trials)

timing, the elapsed time is the longest in the frame, so the possibility of error is higher than for an index with an early transmission timing. As mentioned above, even if the index with the late transmission timing is selected, no error may occur if the clock drift occurs to cancel out the accumulated clock drift value. However, this paper does not discuss how to set the time synchronization timing of PLIM.

V. CONCLUSION

PLIM and DPLIM, which can be applied to improve the performance of LPWA, were implemented on actual equipment. In order to clarify the impact of clock drift caused by a poor oscillator in the actual devices, this paper confirmed performances of the index demodulation error rate using the sensor node which is implemented PLIM and DPLIM. The experimental results show that the impact of clock drift on PLIM is significant in practical applications, while the impact of clock drift on DPLIM is suppressed. As a result, DPLIM is shown to be useful in actual radio equipment.

ACKNOWLEDGMENT

This research and development work was supported by the MIC/SCOPE #JP235004002. This work was supported by JSPS KAKENHI Grant Numbers JP21K04049.

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