2.4 Gbps Real-Time Visible Light Communication System Based on Blue Laser Diode

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***Abstract*—In this paper, a real-time visible light communication (VLC) based on blue laser diode is implemented on field programmable gate array (FPGA) platform. To reduce requirements for signal processing speed, we propose a parallel scheme for modulation and demodulation with simple hardware implementation and low performance loss. Finally, we successfully constructed a VLC system prototype with 600 MHz transmission bandwidth and 2.4 Gbps communication rate over 1 m link distance. Actual measurements shows that 10^{-5} magnitude bit error rate (BER) is achieved without forward error correction (FEC), which demonstrates excellent performance in reported single-source VLC system.**

***Index Terms*—visible light communication, blue laser diode, real-time, FPGA implementation**

I. Introduction

VLC offers advantages such as rich spectrum resources, high transmission rates, immunity to electromagnetic interference. Under the challenges of rapidly growing communication demand and increasingly crowded spectrum in traditional radio frequency, VLC has received widespread attention and in-depth research, becoming a key technology for future communication in 5G and 6G [1].

VLC has enormous potential in various application scenarios, such as high-speed data transmission, smart lighting, power line communication, intelligent transportation, indoor positioning, and underwater communication [2]. Indoor high-speed communication is an important research direction. There are numerous studies focus on VLC devices, channel modeling, transmission and networking, utilizing various techniques to improve communication rate of VLC.

Light Emitting Diode (LED) is wildly used as light sources due to low power consumption, high luminous efficiency, long lifetime and low manufacturing cost. After simple modification of LED with modulation bandwidth, VLC can utilize the widely deployed LED lighting infrastructure to achieve the integration of lighting and communication, exhibiting advantages of low cost, environmental friendliness and energy efficiency. Bian, Tavakkolnia and Haas presented a 15.73 Gbps VLC over 1.6 m link distance using wavelength division multiplexing (WDM) and orthogonal frequency division multiplexing (OFDM), which is the highest data rate of LED-based system [3]. Compared with LED, laser diode (LD) shows frequency and phase coherence, has larger modulation bandwidth and allows higher speed data rate. Wei et al. demonstrate 40 Gbps VLC system using polarization multiplexed red/green/blue (R/G/B) LDs in 2019 [4].

However, Most studies mainly focus on improving transmission rate of VLC link by off-line signal processing, which cannot be used for real-time communication. Li et al. proposed a time-domain synchronous OFDM (TDS-OFDM) VLC system and reached 544.32 Mbps real-time peak rate in total using RGB-LEDs [5]. To promote application and popularization of VLC in future communication, real-time speed is still needed to be improved to >1 Gbps.

This paper presents the implementation of a 2.4 Gbps real-time VLC system with 600 MHz transmission bandwidth based on blue LD. Two FPGA chips are used to achieve high-speed signal modulation and demodulation, and a VLC experiment prototype is developed with other key devices. After actual test of prototype performance, signal-to-noise ratio (SNR) at the receiver end is about 20 dB and BER is 10^{-5} magnitude at a distance of 1 m visible light link without channel encoding and decoding.

II. System Model

This study selects quadrature amplitude modulation (QAM) single carrier (SC) modulation. Compared to OFDM, SC has lower peak to average power ratio (PAPR). Transmission bandwidth of this system is 600 MHz and total communication rate is 2.4 Gbps by using 16QAM. 4 times sampling rate is needed to meet the Nyquist sampling theorem and simplify signal processing of real-time modulation and demodulation. Table. I presents parameters of this real-time VLC system.

TABLE I: System Parameters

Parameters	Value
Modulation	16QAM single carrier
Transmission bandwidth R_s	600 MHz
Roll-off factor α	0.2
Sampling frequency f_s	2.4 GHz
Intermediate frequency f_c	432 MHz

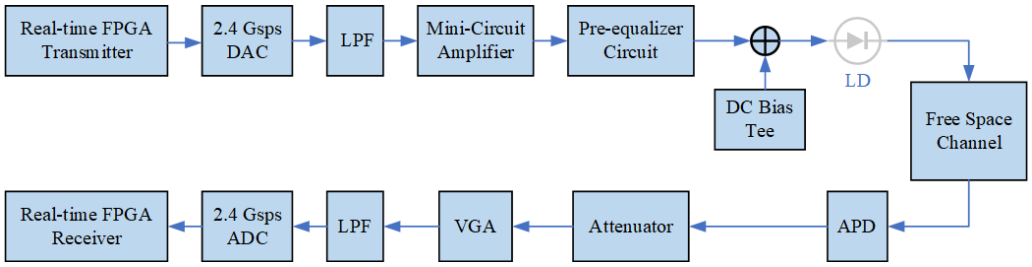


Fig. 1: Block diagram of the real-time VLC system

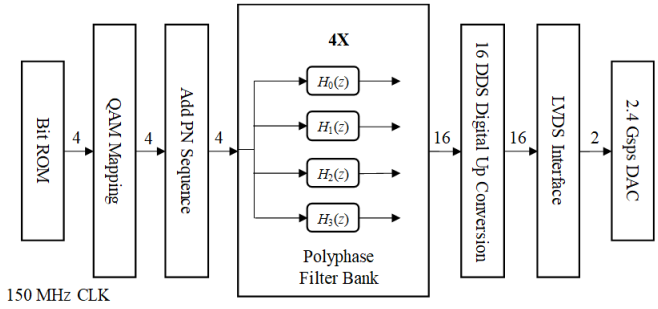


Fig. 2: Block diagram of the transmitter implementation

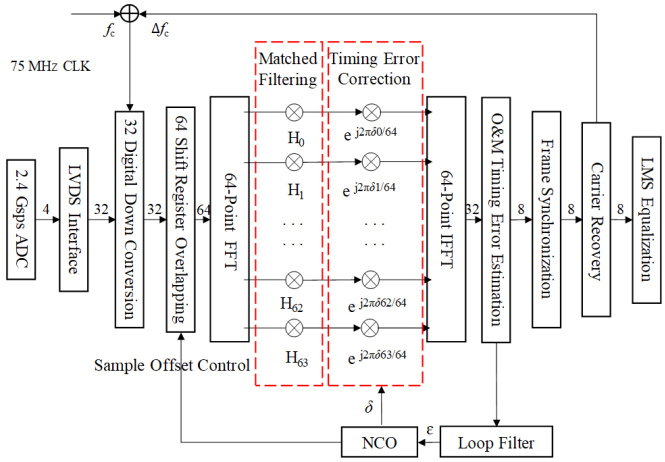


Fig. 3: Block diagram of the receiver implementation

A. Total VLC System Description

Fig. 1 shows block diagram of real-time VLC System proposed in this paper. The FPGA transmitter performs real-time modulation of binary signal and 2.4 Gsps analog-to-digital conversion (DAC, Analog Devices AD9739) converts to analog current. After 1.1 GHz low pass filter (LPF) and Mini-Circuit amplifier, a 1.1 GHz analog pre-equalizer is used to compensate nonlinear distortion from LD and other devices to make spectrum flat. Then bias-tee adds DC bias voltage for driving LD to emit light while the signal modulates the intensity of laser beam. After 1 m free space VLC link, light with signal is directed detected by avalanche photon diode (APD, HAMAMATSU C5658) in the receiver end and subsequently converted to electrical signal. The front-end analog devices consists of attenuator, variable gain amplifier (VGA), LPF and 2.4 Gsps digital-to-analog conversion (ADC, Texas Instruments ADC08300) that samples signal and sends to FPGA, Finally, the FPGA receiver recovers original signal via real-time demodulation.

B. Transmitter Architecture

Fig. 2 shows block diagram of the transmitter implementation. 4 symbols in parallel is read from ROM and mapped to 16QAM constellation. A 64-point known pseudo random (PN) sequence is added for frame synchronization and parameter estimation, followed by 2304 data symbols. To reduce complexity and clock frequency of modulation, we utilize time-domain parallel architecture of polyphase filter. According to Nobel Identity, the system is equivalent after swapping the order of oversampling and filtering. By quadrature multiplexing of polyphase filter bank from multi-phase decomposition of square root raised cosine (SRRC) shaping filter, we obtain 16 band-limited signal outputs. Digital up converter is also based on this parallel structure with 16 direct digital synthesizer (DDS). Finally, symbols modulated in parallel by FPGA are sampled by dual port 2.4 Gsps DAC through low voltage differential signaling (LVDS) interface. Thus, we achieve modulation and transmission of 2.4 GHz sampling rate signal using only 150 MHz FPGA clock.

C. Receiver Architecture

Block diagram of the receiver implementation is illustrated in Fig. 3. We adopt Alternate Parallel Receiver (APRX) architecture, which converts time-domain convolution of matched filtering into frequency-domain multiplication via DFT [6]. 2.4 Gsps ADC performs direct sampling of the intermediate frequency(IF) signal converted by APD and obtain 32 parallel paths by LVDS serial-to-parallel conversion. Then IF signal is transformed to baseband by digital down conversion (DDC) in parallel. Overlap and save method is used to make circular convolution from DFT multiplication equivalent to linear convolution. Thus, 64-point FFT is required after 64-length shift register and multiplied by stored DFT of SRRC matched filter $\{H_0, H_1, ..., H_{63}\}$. Half of the components are directly set to zero to achieve lowpass filtering, thereby saving half of multiplication operations. Subsequently, 32 points of 64-point IFFT outputs are results of matched filter. APRX architecture has identical performance to conventional serial receiver with low implementation complexity and resource consumption.

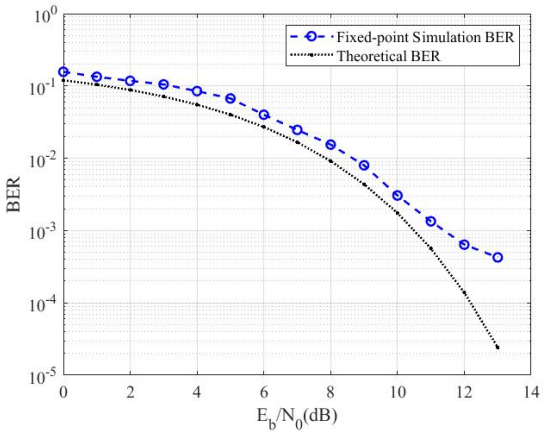


Fig. 4: Simulation BER performance of proposed receiver

Timing synchronization is based on phase locked loop(PLL). The O&M algorithm is used for timing error estimation, which can be described as follows [7]. Calculate the squared envelope of received signal oversampled as N/T rate

$$x_k = \left\| \sum_{n=-\infty}^{n=\infty} a_n g\left(\frac{kT}{N} - nT - \epsilon T\right) + n\left(\frac{kT}{N}\right) \right\|^2 \quad (1)$$

compute the complex Fourier coefficient of L symbols (LN samples)

$$X_m = \sum_{k=mLN}^{k=(m+1)LN-1} x_k e^{-j2\pi k/N} \quad (2)$$

the phase is unbiased estimation of timing error

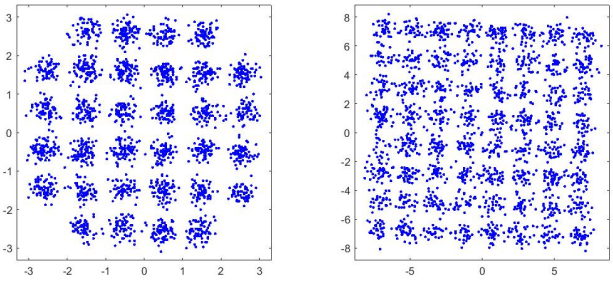
$$\hat{\epsilon}_m = -\frac{1}{2\pi}\arg(X_m) \quad (3)$$

In our implementation, we choose $N = 4$ and (2) can be simplified to addition and subtraction operations. (3) is conducted by pipeline CORDIC algorithm. After loop filter and NCO of PLL, the estimated value is converted into phase factor to correct timing error in frequency-domain according to time-shifting property of the Fourier transform, and sampling point offset is adjusted by controlling shift register address.

Frame synchronization is achieved by performing correlation operations with known PN sequence. The correlation peak of adjacent frames can also be used for carrier frequency offset (CFO) estimation, which Adjusts frequency at the input of DDC by feedback similarly after loop filter and NCO of PLL.

$$\Delta f = \frac{1}{2\pi N_f T_s} arg(R_1^* R_2) \quad (4)$$

In addition, carrier recovery contains carrier phase offset synchronization, which is based on decision feedback PLL by calculating phase difference between the constellation points on the diagonal and their decision values. Finally, Linear Least Mean Square (LMS) adaptive equalization is utilized to eliminate distortion and interference of VLC channel.



(a) (b)

Fig. 5: Simulation results of (a) 32QAM (b) 64QAM

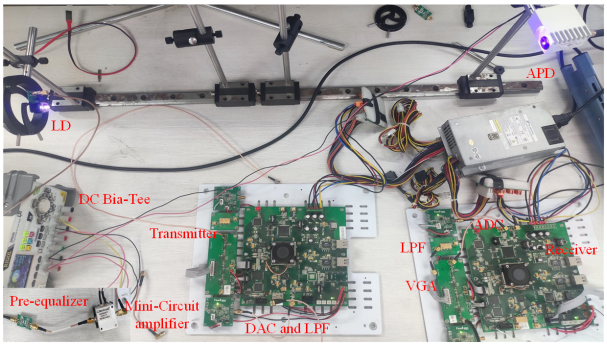


Fig. 6: Photograph of the VLC experimental setup

Based on the parallel receiver architecture proposed above, clock frequency for demodulating the 2.4 GHz sampled signal was reduced to 75MHz. To validate the feasibility of structure and algorithms of proposed receiver and provide guidance for hardware implementation, we conducted fixed-point simulation in MATLAB R2020a. The BER performance is presented in fig.4. Basic parameters have been shown in Table. I, and we add 1/40000 sampling frequency offset and 0.25 initial normalized phase offset. Compared with theoretical results, the BER loss is quite small. Verilog hardware description language (HDL) code is demonstrated and simulated and result is consistent.

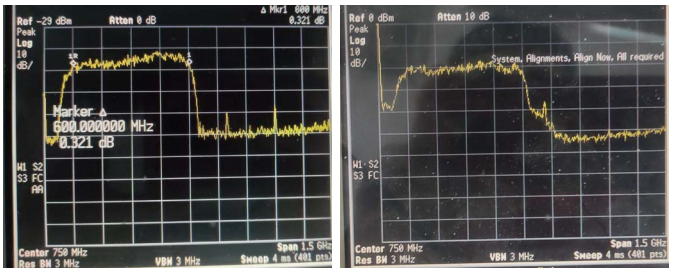
By using high-order modulation such as 32QAM and 64QAM, spectral efficiency is improved and transmission rate reaches up to 3 Gbps and 3.6 Gbps. Constellation diagrams after demodulation simulation are shown in fig.5. The result shows feasibility of further enhancing communication rate in future work. But symbol error can be seen and FEC is necessary for reliability of transmission. Hence we only demonstrate 16QAM VLC system on FPGA with low BER in this paper, and will increase to at least 64QAM after real-time and high-speed low density parity check code (LDPC) is implemented.

III. Implementation Results

After analysis, synthesis and fitter in Quartus Prime 16.1 software, real-time transmitter and receiver are implemented on FPGAs (Intel/Altera Stratix IV EP4SE530H35I3). From the

TABLE II: Resources and Timing Reports

Parameters	Transmitter	Receiver
Combinational ALUTs	27697(8%)	155580(44%)
Total registers	19898	85102
Block memory	3417088(16%)	6078464(29%)
DSP block	64(6%)	1008(98%)
Fmax	166.94 MHz	82.9MHz



(a) (b)

Fig. 7: Frequency spectrum of (a) transmitted signal (b) received signal

resources and timing reports in Table. II, we can see receiver consumes quite more resources than transmitter because of containing more demodulation algorithm like FFT/IFFT and timing synchronization in parallel, and 98% DSP block is used for massive multiplication. Maximum clock frequency (Fmax) of the transmitter and receiver are respectively 166.94 MHz and 82.9MHz, both meeting 2.4 Gbps data rate requirement with 16 paths and 32 paths.

As shown in Fig.6, an experimental prototype is demonstrated with FPGAs and other VLC components. Spectrum in fig.7 illustrates that signal is pre-distorted by pre-equalizer circuit before driving LD, resulting in flat spectrum after APD at the receiver end and SNR is about 20 dB. Real-time constellation output of the implemented VLC system is shown in Fig.8, which is 32 times of normalized constellation after quantization. The signal is successfully demodulated and low BER is achieved via hard-decision demapping without FEC.

Table. III indicates BER at different link distances ranging from 0.3 m to 0.8 m. Three experimental measurements are conducted by transmitting approximately 2×10^7 frames, totaling 2×10^{11} bits each time. Average BER is 10^{-5} magnitude, which exhibits only small performance loss compared to theoretical values.

IV. Conclusion

In this paper, we implement a real-time, high-speed VLC system based on blue LD and FPGA using parallel architecture for modulation and demodulation. The transmission bandwidth is 600 MHz and communication rate reaches 2.4 Gbps using 16QAM. Actual measurements shows that 10^{-5} magnitude BER is achieved without FEC over 1m free space link. Futhermore, we can utilize 64QAM to enhance spectral efficiency and improve communication rate to 3.6 Gbps. To reduce BER and enhance reliability and anti-interference capability

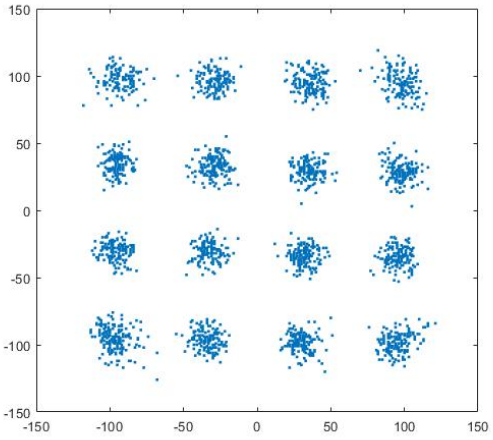


Fig. 8: Real-time constellation of the VLC system

TABLE III: The Measured BER Results

Distance (m)	Experiment Number			Average BER
	1	2	3	
0.3	5.33×10^{-5}	5.05×10^{-5}	5.88×10^{-5}	5.42×10^{-5}
0.4	5.52×10^{-5}	5.02×10^{-5}	6.02×10^{-5}	5.52×10^{-5}
0.5	6.23×10^{-5}	6.30×10^{-5}	6.32×10^{-5}	6.28×10^{-5}
0.6	6.91×10^{-5}	6.44×10^{-5}	6.75×10^{-5}	6.70×10^{-5}
0.7	5.86×10^{-5}	5.89×10^{-5}	6.04×10^{-5}	5.93×10^{-5}
0.8	6.74×10^{-5}	7.57×10^{-5}	7.78×10^{-5}	7.36×10^{-5}

of transmission signal, LDPC code can be applied for error detection and correction.

Acknowlegment

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