Design of a Fault Detection Circuit for One-Time Programmable Memories for Reducing Time

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***Abstract*—** As memory becomes more versatile, testing to detect defects becomes important. Defect testing occurs at various stages of the device's lifecycle to ensure proper functionality and to verify that it meets the specifications determined by the customer. Having a circuit built into the circuit itself to detect faults can ensure accurate and reliable behavior, and eliminate the need for special equipment for testing, reducing costs and saving time. Accordingly, this paper proposes a circuit that can quickly and accurately detect faults in One-Time Programmable (OTP) Memory. The work has been implemented on a TSMC 55nm CMOS process and the OTP Memory is a 256X32bits One Time Programmable Device used in the TSMC 55nm process from eMemory Technology Inc.

Keywords—Fault Detection Circuit, One-Time Programmable Memories(OTP), Verilog HDL

I. INTRODUCTION

One-Time Programmable (OTP) Memory is used when data that requires little or no modification or change needs to be stored permanently. The advantage of OTP Memory is that standard CMOS processes can be used, and simple design allows for high reliability and low power consumption at a low cost [1]. It can also store data permanently, making it a good choice for many applications, such as microcontrollers and embedded systems, if you need to move to a system-on-chip[2].

As the applications of One-Time Programmable Memory become more diverse, fault diagnosis becomes critical [3]. Errors or Faults in memory can be caused by a variety of factors, including manufacturing defects, process variations, environmental factors, or aging. Faulty memory can have serious consequences for applications due to the loss of data. Especially in the case of OTP Memory, a fault detection circuit is necessary because the memory is programmed once and cannot be modified further. In addition, OTP memory has a wide range of read and write latencies. Because each memory has a timing definition that must be respected during operation, a significant amount of test time is required to detect faults without additional circuit design.

Along with the BIST built into the OTP memory itself, having a circuit that can detect faults outside of the memory will allow for more accurate recognition of faults and redundant compensation. Fault detection circuit can verify that the memory is operating correctly and stably, and ensures accurate and reliable operation for the life of the memory. The fault detection circuit allows to compare the output of a memory cell to its expected value, and the output signal informs the system or operator that the memory is unreliable. Including fault detection circuit in the design is critical for many applications because it enables errors to be detected before serious damage is done. The circuit also allows for faster detection of faults, which can significantly save time and cost in chip testing.

As detecting faults in memory and reducing cost by saving time is important, in this paper we present a digital circuit that can identify the presence of faults or errors in OTP memory cells.

II. ARCHITECTURE OF FAULT DETECTION CIRCUIT

A. Top Block Diagram

In this paper, we have constructed a circuit to check whether the OTP Memory is properly programmed and read. Fig 1. is the Top Block Diagram including Fault Detection Circuit. The OTP memory used in this paper is composed of 256x32-bits and can be accessed by 1 word(4 bytes) by bus operation. As Shown in Fig 2. we have divided the memory into three sections, Analog, Digital_1, and Digital_2, to allow for different uses of the data. The first section is set to store the data required for Analog blocks, and the second and third sections are set to store the data required for Digital blocks, and the size of each section can be determined depending on how it is utilized. Each section is divided into 44 bytes and defined as a page, and the first 4 bytes of each page are marked with a valid flag to check whether the page is a program or not. The total number of Analog pages is 15, Digital_1 pages are 4, and Digital_2 pages are 4. The Register File is also designed to be divided into 3 sections like OTP Memory, and written in a size of 103X8bit to have only one page each for Analog, Digital_1, and Digital_2 sections.

Finally, the OTP Memory Fault Detection circuit presented in this work, which can detect memory faults, is connected to the AHB bus.

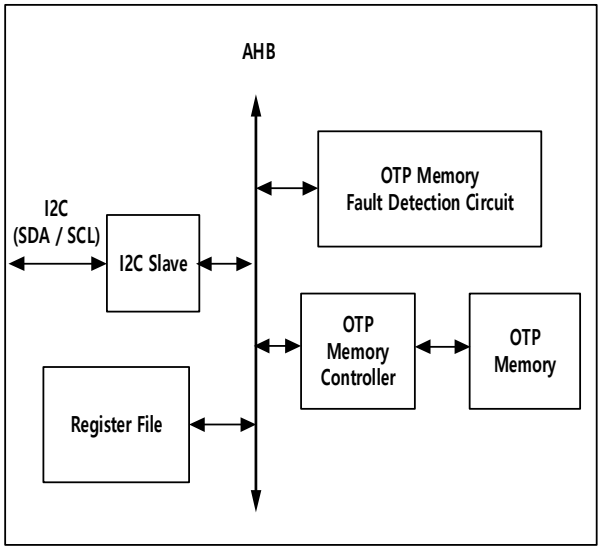


Fig. 1. Top Block Diagram of Fault Detection Circuit

The Fault Detection Circuit not only has the ability to detect faults, but also includes Power On, Power Off, Program, and Read operations so that the OTP Memory can be easily accessed through the circuit. All functions can be activated with a single command, and signals from the Fault Detector can be checked via I2C.

III. Functions of Fault detection

In this section, it describes the functions that can detect the specific default of OTP based on the OTP Fault Detection Circuit presented above. There are four types of logic to check if there is a problem with the OTP.

TABLE I. TYPE OF FAILT DETECTION

Type
Read All
Program Verification
Read Verification
Auto Program on Register File

Table 1. describes the operations for detecting faults that will be presented in the following. In addition, performing the four tasks essentially requires powering on and off the OTP memory and programming/reading the address unit. Therefore, for fault detection, all operations include a power on, power off sequence and may include a program or read operation depending on the situation.

By using multiple functions that can detect faults together, it is possible to simply test whether there is a fault or not when the chip is released, and the time can be extremely reduced compared to the existing read or program operation.

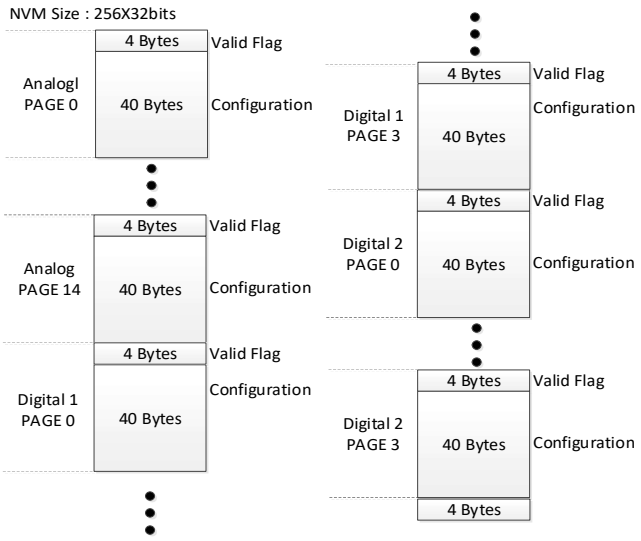


Fig. 2. Section of OTP Memory

A. *Read All Operation*

This operation functions to read data stored at any address in the OTP memory. The default value for the OTP memory we use is 1. Therefore, if nothing is programmed into memory, the OTP should read all F when it is finished. In case there is a problem with a particular address and 0 is read instead of 1, the address is recognized as unusable and faulty.

B. *Program Verification Operation*

When programming into memory, it is essential to make sure that the data is written exactly to the address of what should be the desired data. Since the OTP memory can only be programmed once, it is useful to check that the value stored in the memory is correct before fetching and writing the data to it, to prepare for the event that the data is written incorrectly. We added a function called Program Verification to do it. This behavior first programs the desired value into an address in OTP memory that targets the desired value, and then reads that address back. By reading it back, it can check that the data actually got written. If a value other than the programmed data is read, a fault can be detected.

C. *Read Verification Operation*

Read Verification is to compare the data programmed into the OTP with the Register file, which stores the values needed for the blocks to work. As described above, the Register File, which contains the values that need to be delivered to the Digital Block such as Controller consisting of Digital and the Analog Block such as Analog To Digital Converter (ADC)/Phase Locked Loop (PLL), is continuously updated by the values programmed in the OTP Memory. In this case, it is important to determine which page's OTP Memory the user used. This behavior allows the user to check how much of the OTP Memory has been used, and to compare the Register File to the OTP Memory to determine if it is faulty or not.

The detailed operation is as follows. First, the page information is created at the very beginning of the behavior so

that the user can select the desired page and proceed with the Read Verification operation. Then, the OTP memory reads the programmed value and compares the data in the Register File through the AHB bus with the value read from the OTP memory and gives out the output signal.

D. Auto Program on Register File (AUTO PGM) Operation

The Register File is not only accessible from the OTP Memory, but can also write data using communication protocols such as I2C or SPI, causing data to be inconsistent between the OTP Memory and the Register File. To prevent this problem, a behavior is needed to automatically dump the data in the Register File to the OTP Memory. By sending a command to the OTP Memory to program the data in the Register File, it is possible to skip the process of programming the same value as the data in the Register File one by one. After all the values in the register file are written to the OTP memory, compare the imported data with the programmed data to confirm that it worked correctly, and then read the programmed data again to confirm that it was written correctly. Like Read Verification, Auto Program on Register File Operation also sets the page information in advance to dump the register file data to the desired page.

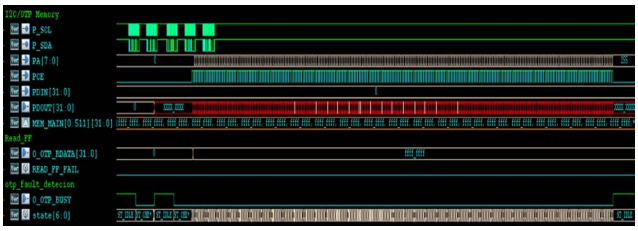
IV. Simulation Result

We synthesized and PNR the designed Default Detection Circuit using tsmc 55nm process. After PNR, we ran Post Simulation with Post NET.

A. Read All Operation

In Fig. 3, (a) is a Read All Operation with no program at all. Since all values are 1, notice that the Fail flag is low. If there is a fault such that the default value of 0 exists, the fail flag will be high to detect the fault. In (b), a random value is programmed into Analog Page 0 and then a Read All operation

(a)



(b)

Fig.3. (a) Waveform of normal Read All Operation before program (b) Simulation of programming data into Analog Page 0 and then doing Read All Operation

is performed. A fail flag is raised at the address where the program was programmed, and if the flag is raised, it tells the program what part of memory it was programmed in from the beginning. This can be utilized to reduce chip test time by not having to access and read the addresses in the OTP memory one by one. The time to read the address of all OTP memory is 1.2s, but with this behavior, it takes 21.6ms to check the fault of OTP memory.

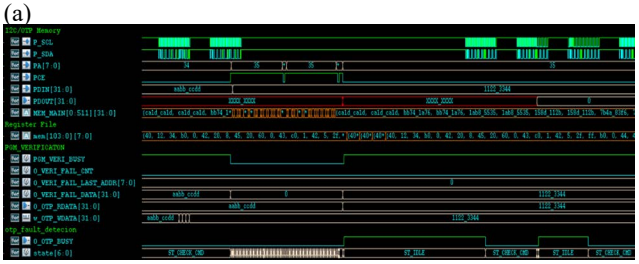
B. Program Verification Operation

Fig. 4 is about Program Verification. Fig. 4 (a), after programming 32'h11223344 data to address 35 of OTP Memory, the programmed value is read properly. In (b), 32'hca1dca1d was arbitrarily forced to 32'hffffffff, which is different data, to the programmed address. If the programmed value is different from the read value, a flag is raised that the value failed with the address value of the part where the value is different. By using Program Verification instead of Program/Read, it is possible to verify the correct value in a short time and intuitively find the fault.

C. Read Verification Operation

Fig 5. compares the data programmed in the OTP with the data updated in the Register File. Page is set to enable read verification for only Analog Page 3 and Digital_2 Page 2. Analog Page 3 does not display the analog_fail flag because the data in the OTP Memory and the data in the Register File are the same. However, in the latter case of reading Digital_2 Page 2 from the OTP memory, which is different from the value stored in the Register File, digital_2_fail is shown with the failed address.

(a)



(b)

Fig. 4. (a) Waveform of normal Program Verification Operation (b) Simulation of different programmed and read values

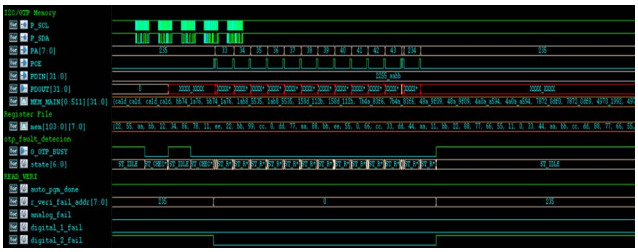


Fig. 5. Waveform of Read Verification Operation

D. Auto Program on Register File(AUTO PGM) Operation

The Auto Program on Register File Operation is shown in Fig 6. Page is set to Analog Page 6 and if this operation is executed, the values in the Register File from address 66 to address 76 of the OTP memory are dumped and programmed. For example, it can be seen that 32'haabbccdd, which was in Register File [1], is programmed into OTP Memory [66] exactly the same. After executing AUTO PGM, running it with Read Verification, the value in the register file can be checked if the memory is written properly.

V. CONCLUSION

This paper presented a circuit that detects faults inherent in OTP memory. By using a fault detection circuit, it reduces the time it takes to find faults in OTP Memory and makes the data stored in the memory array more accurate and reliable. By utilizing this, the time to test a chip when it comes out can be dramatically reduced, and with the reduction in time comes a reduction in cost.

Fig. 6. Waveform of Auto Program on Register File Operation

ACKNOWLEDGMENT *(Heading 5)*

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