A Design of Phase Shifting Phase Locked Loop with Dual Loop Structure for Beamforming Application

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***Abstract*— This paper presents a structure of Phase-Locked Loop (PLL) that can shift phase by itself. The frequency of the reference clock is 50MHz, and the target frequencies are 5.8 GHz and 4.8 GHz. The PLL structure in this paper has one more Phase-Frequency-Detector (PFD) and one more charge pump. The key idea is to apply two divider output signals with constant delay to each PFD and Charge Pump, then the phase of the output signal of Voltage-Controlled-Oscillator (VCO) is shifted depending on the current of two charge pumps. In this paper, the circuit was designed using a 130nm CMOS process. The phase shifting resolution of the designed PLL is 5.625 degrees.**

Keywords— Phase-Locked Loop (PLL) ; Phase Shifting Phase-Locked Loop; Beamforming;

I. INTRODUCTION

Beamforming is a key technology in AI wireless charging transmission technology. In general, beamforming is implemented in a structure in which a phase shifter is added before Power Amplifier (PA). Therefore, an additional area for phase shifter is required, and the losses of each block are gathered and make it difficult to operate efficiently. This disadvantage may be solved by making the PLL shift the phase by itself, and it can be implemented by simply adding one current mirror cell [1].

In this paper, we would like to introduce a structure with higher degree of freedom for phase shifting PLL. Phase shifting PLL presented in this paper has the advantage that the PLL do phase shift by itself, so an additional phase shifter is not required. To implement this structure, one PFD, and one charge pump, are added compared to the general PLL structure, and some logic cells that generate some specific delay.

A simple phase shifting process is as follows. Two PFDs receive Divider output signals with a constant delay interval as input, and the amount of shifted phase is determined by the current of the charge pump connected to the PFD that receives the lagged signal. Eventually, by controlling the charge pump current, it is possible to shift as much phase as desired.

In section 2, we will explain the phase shifting PLL structure proposed in this paper and the principle phase shifting. In section 3, we will explain the structure and operation or the sub-block, and the layout and simulation results will be shown in section 4.

II. ARCHITECTURE

A. Top Block Diagram of PLL

Fig. 1 is the Top Block Diagram of Proposed PLL. This Phase Shifting PLL requires one more PFD and one more CP, and an additional 4TVCO_GEN cell composed of logic gates that can produce two signals with a constant delay of 4 times the period of VCO output (TVCO).

PLL in this paper receives 50MHz signal as a reference clock, and the target frequencies are 5.8GHz and 4.8GHz. PFD1 and PFD2 have same structure and PFD2 gives reset (RST) signal to PFD1. CP1 receives the generated signals form PFD1 and CP2 receives input signals from PFD2. Charge pump current which is sum of current of CP1 (Icp1) and current of CP2 (Icp2) is 320uA for this paper. DC current is provided to the Loop Filter (LF) to prevent the lock state from changing while shifting phase. For the LF, second order LF is used because this PLL is integer type, so it is not necessary to use a higher order of LF. The C1 value of LF is 60pF, C2 value is 800pF, and the R2 value is 6KOhm. PLL with this LF values has a bandwidth of 309kHz and a phase margin of 48.92 degrees in 5.8GHz operation mode, and a bandwidth of 197kHz and a phase margin of 56.42 degrees in 4.8GHz operation mode.

LC VCO is designed to cover both frequencies of 5.8GHz and 4.8GHz. To divider the output signal of VCO by 116, divider chain which is composed of current-mode-logic (CML) divider, True-Single-Phase-Clock (TSPC) frequency divider, and programmable divider is used. Additional logic parts are added to de phase shifting operation, and it makes FDIV1 and FDIV2 signals which enter PFD1 and PFD2.

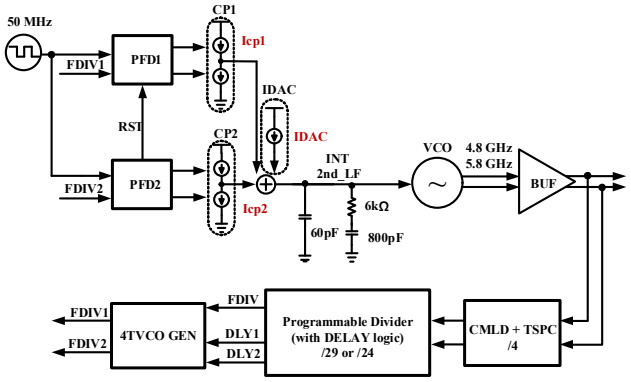

Fig. 1. Top block diagram of phase shifting PLL

The operating principle of phase shifting is as follows. In the 4TVCO_GEN cell, two signals having a constant delay are generated based on the divider output. A constant delay amount between these two signals is 4 times TVCO. In order to generate a signal with a delay difference of 4 times TVCO, a Dual-modulus divider inside the divider produces a signal with a delay difference of 4 times TVCO. Among the two signals generated from the 4TVCO_GEN, the leading signal enters PFD1 and the lagging signal enters PFD2. The UP and DN signals created by PFD1 and PFD2 enter the inputs of CP1 and CP2, respectively. Sum of the ICP1 and the ICP2 is a constant value, and the amount of phase shifting is determined according to the ratio of ICP2 to the value of sum. The exact equation for the amount of phase to be shifted is as follows.

$$\text{The amount of shifted phase} = [(TXO * IDAC) / (TVCO * ICP) + (ICP2 * TXO) / \{ICP * (TVCO / 4)\}] * 360 \quad (1)$$

In the Equation (1), TXO is the period of the reference clock, TVCO is the period of the VCO output signal, and I_{CP} is the the of ICP1 and ICP2. The PLL in this paper is designed such than ICP2 increases by 1.25uA for one-bit changes, and the ICP value is 320uA, so it has a phase shifting resolution of 5.625 degrees per bit.

Additional Current mirror cell is used for giving DC current to make sure that only DN signal is generated from PFD to CP after lock is done. This part is just added to fix the state after PLL is locked.

III. Building Blocks

A. Voltage Controlled Oscillator

Fig. 2. is a structure of VCO used in this paper and it has a basic LC VCO structure. Four varactors are used, and a bias voltage is set to the varactor node closed to the VCO output side so that the linear part of the varactor capacitance can be used. It also uses discrete capacitor bank that can be controlled by digital bits to increase the overall value of capacitance vertically. At this time, after designing a capacitor bank to cover 5.8 GHz in process-voltage-temperature (PVT) variation, one digital bit and one capacitor bank are additionally added to cover 4.8 GHz. The value of this capacitor bank is set to be enough to cover 4.8 GHz in all corner cases of PVT variation.

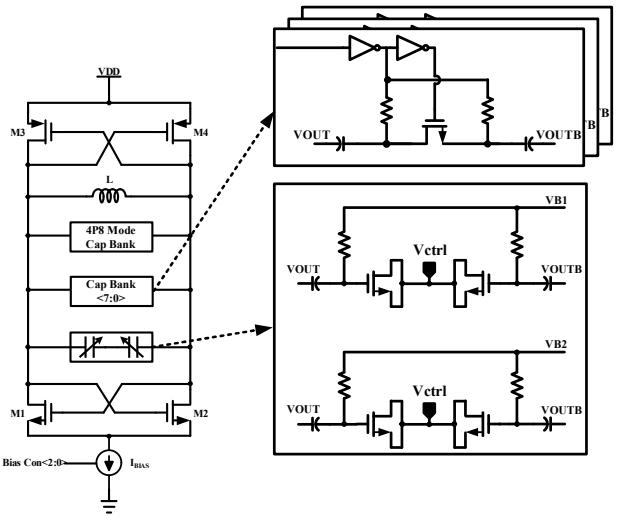

Fig. 2. Schematic of LC VCO

This VCO has a gain of VCO (KVCO) value of 153.3 MHz/V for 5.8 GHz operation and 95 MHz/V for 4.8 GHz operation based on TT/40 degrees. In addition, for the same condition, phase noise at 1MHz offset frequency is -112.45dBc/Hz for 5.8GHz operation and a -113.02dBc/Hz for 4.8GHz operation.

B. Phase Frequency Detector

Fig. 3. is a structure of PFD used in this PLL. In this PLL, there is no need to consider the dead zone problem because only DN signal will be generated from PFD for enough time by using additional IDAC cells. Therefore, the reset delay to solve the dead zone problem can be removed so that the current mismatch when the UP and DN signals are simultaneously generated would not affect the PLL. In addition, SR latch is added to the output terminal to make it more clear that only one of the UP and DN signals occurs.

C. Charge Pump with IDAC Cell

Two charge pumps are used for this PLL. The structure of two charge pump is same, and Fig. 4. is shows the structure of the charge pump. This charge pump is designed with current mirror and switches using unity-gain-buffer (UGB) and it receives 5uA as a bias current for current mirror. UGB is designed with rail-to-rail folded cascode amplifier which has unity gain bandwidth as 179.4MHz. The current mismatch could be reduced by keeping the voltages of the VCP node and the VUGB node constant using UGB. Also, a cascode current mirror is used to provide a more stable current.

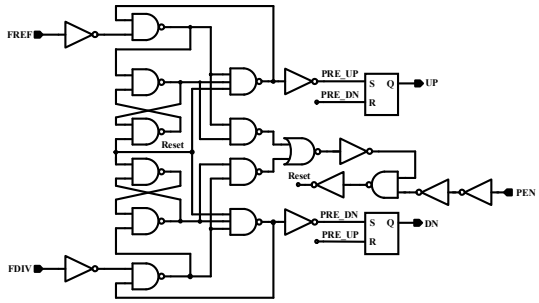

Fig. 3. Schematic of PFD

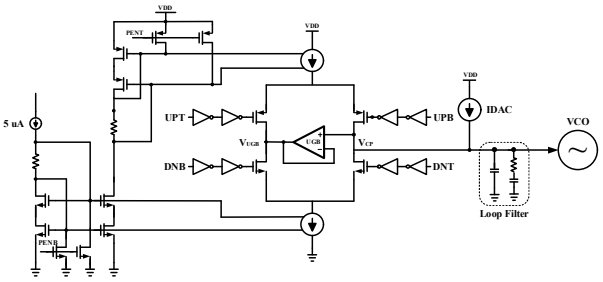

Fig. 4. Schematic of Charge pump with IDAC cell

Let the charge pump receiving the leading divider output signal is CP1, and the charge pump receiving the lagging divider output signal is CP2, and the charge pump currents of each charge pump are ICP1 and ICP2. The sum of ICP1 and ICP2 is constant at 320uA, and the ratio of ICP2 to the sum of two currents determines the amount of shifted phase. So, ICP1 and ICP2 are controllably designed. Each Charge pump uses 9 control bits for UP current and 9 for DN current, that is, a total of 18 control bits. So, it is possible to control the current in detail, and ensures sufficient margin for phase shifting.

An IDAC cell was added to ensure that only DN signal is generated after PLL is locked. It was configured using a current mirror cell with 3 bits assigned to the control bit. In the process of shifting the phase by changing currents of two charge pumps, if the UP or DN signal which is turned on in the lock state changes, the linearity of the phase shifting result will be broken. To prevent this situation, for this PLL, only DN signal is allowed to occur at the locked state.

D. Divider with Additional TVCO/4 GEN Cell

Fig. 5 shows the divider chain used in this paper. In order to divide the high frequency input signal of 5.8GHz, the CML divider which has fast response time is used to divide it by 2 to generate a 2.9GHz signal. Next, to divide the 2.9GHz signal, which is still too fast, TSPC frequency divider is used to divide it by 2 once again. A 1.45 GHz signal produced using a CML divider and a TSPC frequency divider divided by 29 using a programmable divider. Among the programmable divider components, the dual-modulus divider that divides 4 or 5 is composed of TSPC D Flip-flop because the input signal is still relatively high, and the Pulse counter and swallow counter are composed of static D Flip-flop. Finally, the total divider chain makes the output signal of 50MHz.

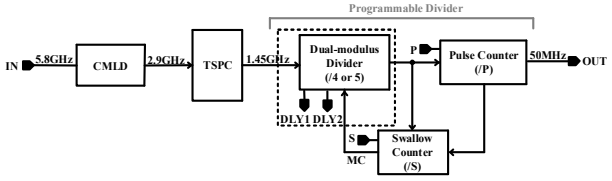

Fig. 5. Top Block Daiagram of the Divider Chain

Now, let me explain the structures which are added to implement the phase shifting operation to this PLL. Fig. 6. Is the schematic of the Dual-modulus Divider. First, three D Flip-flops were added to the output of the Dual-modulus divider. By using the output of the Dual-modulus divider as an input signal and listing three D Flip-flops triggered according to the CLK in series, DLY1 and DLY2 signals are produced, which are two signals with delay differences of CLK period. Since the CLK signal used for this D Flip-flops is an output signal of the TSPC frequency divider at the front end, it is a signal which a 4 times TVCO. Therefore, the DLY1 signal and DLY2 signal have a delay difference of 4 times TVCO. Here, since the set-up time and hold time of the D Flip-flop which makes DLY2 signal are guaranteed, it may be ensured that the DLY2 signal has a constant time interval with the DLY1 signal. The last D Flip-flop is used as a load to make the rising times of DLY1 and DLY2 signals equal.

Next, the TVCO GEN cell show in the Fig. 7. is used to implement the phase shifting operation to this PLL. The purpose of this cell is to create two signals, FDIV1 and FDIV2 which have the same waveform with FDIV signal and have a delay difference of as much as 4 times TVCO. So, it has two input signals of DLY1 and DLY2 which have delay difference of 4 times TVCO to the Clock of D Flip-flops. Also, in order to offset the delay caused by logic cells other than Flip-flop among the programmable divider internal components, the same delay line is constructed with logic cells to create same amount of delay. By putting the Delay Line into the clock of the D Flip-flop, the output of the two DFFs has a time difference between DLY1 and DLY2, that is, a delay of 4 times TVCO. At this time, the last D Flip-flop was used as a load to make the rising time of the FDIV1 signal and the FDIV2 signal equal. The leading signal FDIV1 enters PFD1, and the lagging signal FDIV2 enters PFD2, making this PLL capable to shift phase.

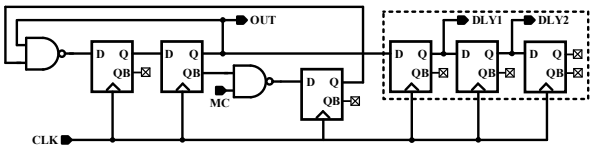

Fig. 6. Schematic of the Dual-modulus Divider

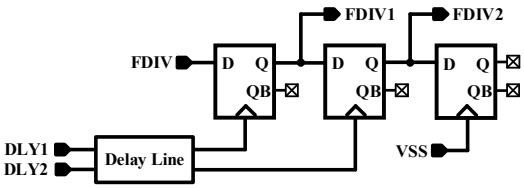

Fig. 7. Schematic of the TVCO GEN

IV. Experimental Results

A. Layout

Fig. 8. is the layout of proposed PLL Top. It is designed with 130nm CMOS Process. The total area of this Layout is 2.298mm * 1.229mm.

B. Simulation Results

Fig. 9. is the Fast-Fourier-Transform (FFT) simulation result of proposed PLL Top. This PLL Locked at 5.8GHz with -4.98dBm and the power difference between target tone and reference spur is 58.5dB.

Fig. 10. is the phase shifting simulation result of this phase shifting PLL. Simulation is done by 4 bits resolution, which can shift 22.5 degrees. The maximum offset of the simulation results with ideal values is 2 degrees.

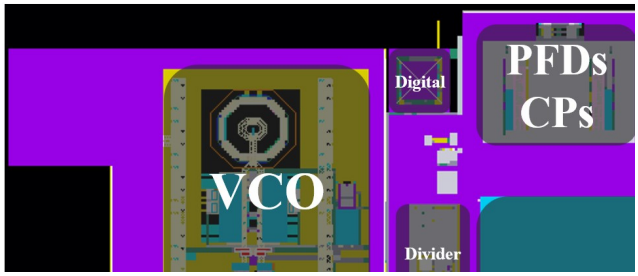

Fig. 8. Top layout of proposed PLL

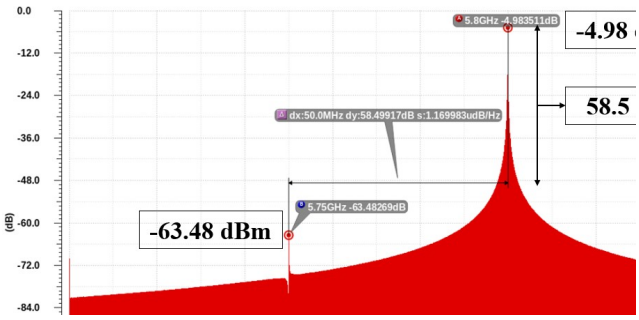

Fig. 9. FFT simulation result of proposed PLL

Table 1. shows the ideal value and simulation result of phase shifting simulation. And Fig. 11. Is the graph of shifted phase, according to the control bits of ICP2. It shows that the result of phase shifting simulation is linear. Yellow curve is ideal value and green curve is real value of simulation result. As shown in the graph, the result has overall linearity and it is almost identical to the ideal value.

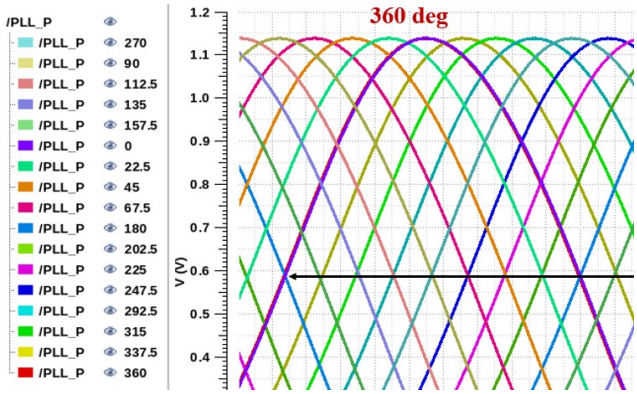

Fig. 10. Phase shifting Simulation result

TABLE I. Phase Shifting Simulation Results

CP Offset	*Ideal*	*Real*
1	0	0
5	22.5	22.84
9	45	45.22
13	67.5	68.43
17	90	90.02
21	112.5	113.75
25	135	134.72
29	157.5	159.36
33	180	180.01
37	202.5	203.79
41	225	226.42
45	247.5	248.69
49	270	270.97
53	292.5	294.3
57	315	317.05
61	337.5	337.4
65	360	360.8

Fig. 11. Shifted phase according to the control bits

V. CONCLUSION

This paper shows the structure of phase shifting PLL which can shift phase itself. It is implemented by adding one PFD, one charge Pump, some logic cells to make delay, and digital bits to control the current of two charge pumps. The added circuits do not occupy a large area compared to the total area, but only adding these parts to a typical PLL structure, the PLL can shift the phase on its own.

In addition, the PLL in this paper is designed to have a phase shifting resolution of 5.625 degrees, but it is also possible to design a phase shifting PLL with more granular resolution by reducing the amount of current changing per control bit of the delay interval of divider output signals entering PFDs.

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REFERENCES

[1] D. Mittal, V. Verma, “Design of Charge Pump Circuit for PLL Application: A Review.” International journal of engineering research and technology 4 (2015)

[2] G. D’Amato, G. Avitabile, G. Coviello and C. Talarico, "DDS-PLL Phase Shifter Architectures for Phased Arrays: Theory and Techniques," in IEEE Access, vol. 7, pp. 19461-19470, 2019, doi: 10.1109/ACCESS.2019.2895388.