Soft-Error Injection System for Processor on FPGA Platform

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***Abstract*—** This paper presents a soft-error injection system on the FPGA platform using an ARM Cortex-M3 processor. The system consists of an error injector that generates random numbers using a Fibonacci linear feedback shift register to introduce errors into an application program status register. The efficacy of the soft-error injection system is assessed and validated on an FPGA platform employing Xilinx XCKU115. Additionally, a user interface is created to configure and test the error-injection system. The system is capable of simulating both single-event transient and single-event upset errors, and it can determine the error duration before returning to the previous error-free state. The soft-error injection system is a valuable tool for evaluating the dependability of embedded systems used in industries such as automotive, industrial control, and consumer electronics.

Keywords— soft error; error injection system; error endurance system; single event upset; single event transient

I. INTRODUCTION

In 1979, it was first reported that semiconductor devices could be affected by alpha particles and cosmic rays [1, 2]. While these particles typically don't cause permanent damage, any resulting errors are referred to as "soft" errors [3]. The frequency at which these errors occur is known as the soft error rate (SER) [4]. Since then, a significant amount of research [5-11] and development has been dedicated to reducing the impact of soft errors on semiconductor devices. Soft errors refer to transient or intermittent errors that occur in digital circuits, typically caused by radiation or other environmental factors. Soft errors can cause incorrect results or system failures, posing a significant challenge to the reliability of processors and other electronic devices. As processor technology continues to advance and electronic devices become more ubiquitous, ensuring processor stability has become increasingly important.

The necessity of processor stability cannot be overstated, as soft errors can have serious consequences in a wide range of applications. From aerospace and defense to healthcare and finance, many industries rely on the reliability of electronic devices to ensure safety and prevent catastrophic failures. As such, ensuring processor stability is crucial for both economic and societal reasons. Moving forward, continued research into verification methods and fault-tolerant designs will be essential for improving processor stability and ensuring the reliability of electronic devices.

This paper presents a soft-error injection system for an ARM Cortex-M3 on a FPGA platform. The system can analyze and evaluate the soft-error vulnerability of the processor. The remainder of this paper is organized as follows. Section II provides the soft-error injection system and Cortex-M3. Section III presents an evaluation environment of the soft-error injection system and its user interface (UI) for system applications. Finally, the conclusion is drawn in Section IV.

II. SOFT-ERROR INJECTION SYSTEM

Fig. 1 shows the soft-error injection system on the FPGA platform. The system consists of error injectors and an ARM Cortex-M3 processor. The error injector generates a single event error and stores its information in a log memory. The Cortex-M3 is widely used in embedded systems, such as automotive, industrial control, and consumer electronics. Thus, we select Cortex-M3 to verify and evaluate the error injection system.

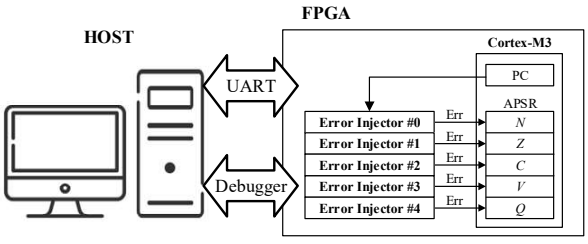

Fig. 1. Soft-error injection system.

A. Error Injection Module

The ARM Cortex-M3 [12] is a 32-bit reduced instruction set computing (RISC) processor, which means that it uses a simplified instruction set to improve performance and reduce power consumption. An application program status register (*APSR*) is a register available on the ARM Cortex-M3 processor that stores the current execution state of the processor.

The *APSR* is a crucial component in processors that stores information about the current state of the processor, such as the

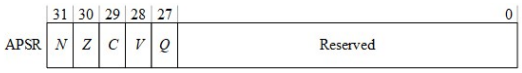

Fig. 2. *APSR* register.

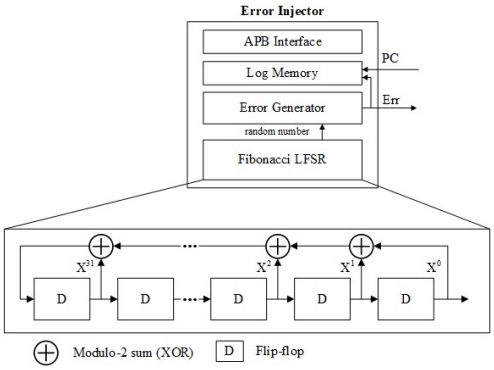

Fig. 3. Error Injector Block Diagram.

program status, interrupt status, and condition code flags. Since soft errors can potentially corrupt the data stored in *APSR*, evaluating the reliability of the *APSR* is essential for ensuring the overall stability of the processor. To achieve this, an error injection system can be utilized to inject errors into the *APSR* and evaluate the effects of these errors on the system performance. Fig. 2 shows the *APSR* register.

- *N* : Negative condition flag
- *Z* : Zero condition flag
- *C* : Carry condition flag
- *V* : Overflow condition flag
- *Q* : Overflow or saturation flag

The soft-error injection system can be used to evaluate the reliability of the *APSR* by generating and injecting soft errors into the register. The system can then monitor the processor's behavior and collect data on the effects of the errors on the overall performance of the processor. By evaluating the results of these benchmarks, researchers can identify potential weaknesses in the processor's design and develop strategies for reducing the impact of soft errors on the system performance.

Error Injection Module

Fig. 3 shows an error injector, which consists of a Fibonacci linear feedback shift register (LFSR), an error generator, a log memory, and an advanced peripheral bus (APB) interface. The error injector is designed as an APB slave.

To design a random number generator for injecting errors at arbitrary times, a Fibonacci LFSR was used, with a feedback polynomial as below

$$P(x) = x^{31} + x^{22} + x^2 + x^1 + 1 \quad (1)$$

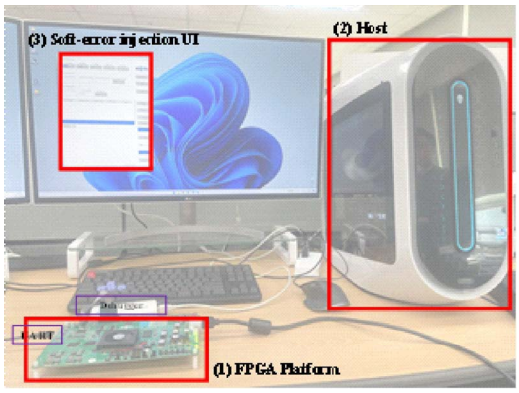

Fig. 4. Evaluation environment of the soft-error injection system.

Soft errors are a type of error that can occur in electronic systems due to the impact of alpha particles or cosmic rays on semiconductor devices. These errors are classified into two types: Single-Event Transient (SET) and Single-Event Upset (SEU). SET errors are temporary, while SEU errors persist as an error state until the system is reset or corrected. In order to evaluate the reliability of electronic systems and improve their resilience to soft errors, it is necessary to support both SET and SEU errors for soft-error injection.

To support soft-error injection, the error injection circuit includes a feature that sets the duration of the error and returns to the previous error-free state once the duration has elapsed. This feature is implemented in the error generator block, which generates errors within the desired duration range using APB to set the range and the generated random number using the Fibonacci LFSR to select a value within that range. The error injection circuit also includes a log memory that stores information about the error occurrence, such as the program count (PC) value at the time of the error and the error duration. This information can be analyzed to identify potential vulnerabilities and improve system reliability.

The ability to simulate soft errors through soft-error injection is critical for evaluating the reliability of electronic systems used in industries such as automotive, industrial control, and consumer electronics. By supporting both SET and SEU errors and generating errors within a desired duration range, the error injection circuit can be used to evaluate the resilience of electronic systems to soft errors. The log memory stores information about the error occurrence, which can be analyzed to identify vulnerabilities and improve system reliability. Ultimately, soft-error injection is an important tool for ensuring that electronic systems are reliable and resilient to the impact of alpha particles and cosmic rays.

III. Verification and Evaluation on FPGA Platform

Fig. 4 shows an evaluation environment of the soft-error injection system using the FPGA platform with Xilinx XCKU115. The environment to demonstrate the soft-error injection system is comprised of three components: (1) the FPGA platform with XCKU 115, (2) a host system to debug using ULINK-pro and communicate on UART, and (3) a soft-

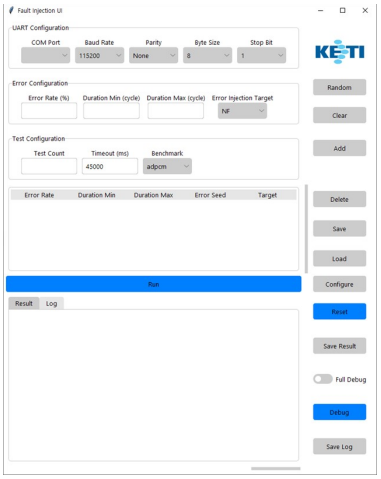

Fig. 5. Soft-error injection UI.

error injection UI. The FPGA platform implemented the error-injection system shown in Fig. 1.

To configure and evaluate the error-injection system, a soft-error injection UI as shown in Fig. 5 was developed using Python 3.6 with Tkinter, pyserial 3.5, and PyInstaller 4.10. The *Error Configuration* tap can set the error rate, duration, and target *APSR* register for soft-error injectors.

- *Error Rate* : Probability of a soft-error occurring for the selected target register.
- *Duration Min* and *Max* : Clock cycle of error persistence when an error occurs.
- *Error Injection Target* : Select *APSR* to inject error (*N*, *Z*, *C*, *V*, and *Q*).

In the *Test Configuration* tap, a user can configure benchmark execution settings for error injection tests.

- *Test Count* : The number of run of the benchmark.
- *Timeout* : Value to prevent a freeze state due to a soft-error when running a benchmark, and the minimum timeout time is displayed according to the benchmark selection.
- *Benchmark* : SNU Real-Time Benchmark *(adpcm, bs, crc, fft1, fft1k, fibcall, fir, insertsort, jfdctint, lms, ludcmp, matmul, minver, qsort, qurt, select, and sqrt)*.

After configuring the benchmark execution settings, the user can initiate the test by clicking the *Run* button. The host then configures the information set by the user interface on the FPGA platform, including the error injection parameters. During benchmark execution, the system reads benchmark results and the final Corex-M3 states to evaluate the impact of soft errors on the stability of the processor. This allows users to assess the reliability of embedded systems and identify potential vulnerabilities that may need to be addressed.

IV. Conclusion

This paper presents the soft-error injection system on the FPGA platform using an ARM Cortex-M3 processor. The system includes an error injector, which uses a Fibonacci linear feedback shift register to generate random numbers for injecting errors in the *APSR*. The soft-error injection system was evaluated and verified on an FPGA platform using Xilinx XCKU115 and a soft-error injection UI was developed to configure and evaluate the error-injection system. The system can support both single-event transient and single-event upset errors, and it can set the error duration and return to the previous error-free value after that duration. Overall, the soft-error injection system provides a means to evaluate the reliability of embedded systems, such as automotive, industrial control, and consumer electronics.

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