A 1.4mW Sigma Delta ADC with Configurable Filter for Sensor Applications

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***Abstract*—**This paper presents a second order Sigma-Delta (SD) Analog-to-Digital Converter (ADC) is designed to achieve low power and high resolution in sensor applications. To reduce the power, CIC filter has been implemented as decimation filter. The digital filter's decimation factor can be adjusted, allowing it to be reconfigured for use with various data rates and input signal bandwidths. The proposed SD-ADC consists of Input Multiplexer, Input Buffer, Current Generator, Reference Generator bias, Common Mode Voltage generator, Clock divider, ADC Core and Digital Decimation Filter. The proposed SD-ADC has an Effective number of Bits (ENOB) of 15.2 bits and Signal to Noise and Distortion Ratio (SNDR) of 80.6 dB. The designed SD-ADC is implemented with 0.13µm Technology using 1.5V power supply and consumes 0.94 mA of current with input frequency of 1 kHz.

Keywords—Sigma-delta ADC; High resolution; Digital Decimation filter

I. INTRODUCTION (*HEADING 1*)

Analog-to-digital converters (ADCs) are essential components in many digital systems that require the conversion of continuous analog signals into digital representations for processing, storage, and transmission. The demand for high-resolution ADCs has been on the rise in various applications, such as audio and video processing, medical imaging, and wireless communications. The capability of achieving high-resolution and high-accuracy conversion with a simple architecture has garnered significant attention for SD-ADCs [1].

SD-ADCs use a feedback loop with a delta-sigma modulator to oversample the input signal and quantize the difference between the input signal and a high-frequency feedback signal. The oversampling and noise shaping process of the modulator enables the use of low-resolution quantizers, while achieving high effective resolution [2]. This makes sigma-delta ADCs suitable for applications that require high resolution.

The resolution of a sigma-delta ADC is a critical parameter that determines its performance. The definition of resolution pertains to the utilization of a certain number of bits for the representation of the input signal. Higher resolution ADCs can represent the input signal with greater accuracy but require more complex circuitry. Therefore, careful consideration of various factors such as the oversampling ratio, the noise shaping filter, the quantizer resolution, and the digital correction techniques is required to tackle the challenging task of designing the high-resolution sigma-delta ADCs. This paper presents a second order discrete-time SD-ADC with ENOB of 15.2 bits and SNDR of 80.6 dB designed for sensor applications. The proposed ADC Consists of 2nd order SDM and Digital Decimation filter.

II. PROPOSED STRUCTURE

A. Top Block diagram of Sigma-Delta ADC

A simplified top block diagram of the proposed SD-ADC is shown in Figure 1. The Proposed SD-ADC consists of a Sigma-Delta Modulator (SDM) and a Digital Decimation filter. A second order Discrete-Time (DT) SDM with Cascaded Integrator Feedback (CIFB) structure [3] is used to guarantee superior stability performance and minimal area. The modulator generates a noise-shaping effect on the accumulation of the signal at the modulator's output. The noise-shaping effect shapes the quantization noise into higher frequencies.

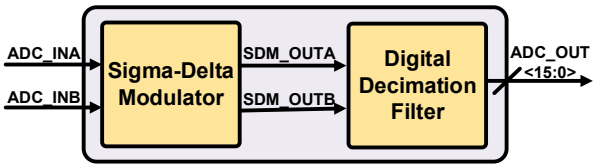

Fig. 1. Block Diagram of SD ADC

B. Block Diagram of 2nd Order Sigma-Delta ADC

Figure 2 presents the block diagram of the 2nd-order SDM. The modulator comprises two switched capacitor integrators, whose output is fed back to integrators [4]. A feedback value of ¼ creates a transfer function for noise-shaping, while a feedback value of 1 ensures that the output from the quantizer tracks the input. This modulator topology offers some noise-shaping ability but a higher overload level, making it ideal for expanding the dynamic range in a low-range environment.

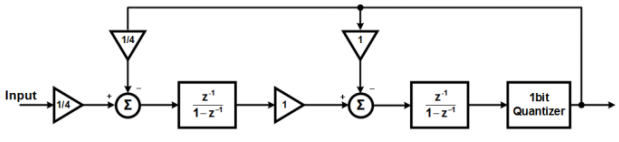

Fig. 2. Block Diagram of 2nd Order SD ADC

C. Block Diagram Sigma Delta Modulator

Figure 3 presents the block diagram of the Sigma Delta Modulator, which converts the signal at a specific sample rate. The feedback loop of the modulator incorporates a 1-bit DAC that operates at the same sample rate as the inputs of two integrators. A noise-shaping effect is generated at the modulator's output. The noise shaping effect shapes the 1-bit conversion quantization noise into higher frequencies. The SD-ADC comprises Input MUX, Current Generator, Voltage Generator, Voltage Reference Generator, and 2nd order core having two integrators and a comparator.

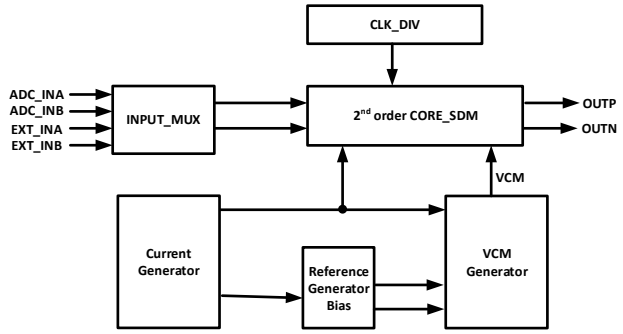

Fig. 3. Block Diagram of Sigma Delta Modulator

D. Proposed Comparator

Figure 4 presents the structure used to construct a single bit quantizer using a dynamic type of comparator. The comparator is followed by two SR-latch cells which determine the outputs of the comparators. This comparator is used for low power and fast response. The comparator offset should be less than ½ of LSB, and the comparator propagation delay should be less than ½ of the Sampling Frequency. The output of the comparator goes to the integrator switches.

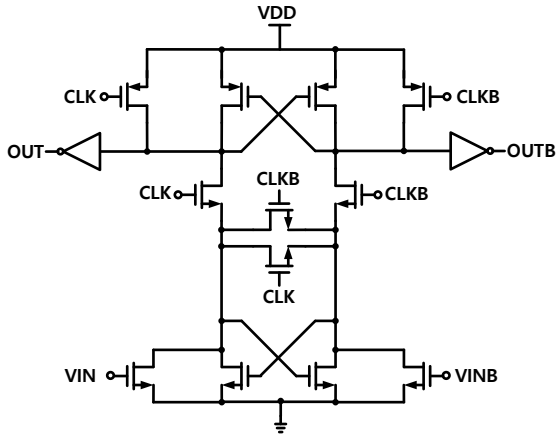

Fig. 4. Proposed schematic of Comparator

E. Proposed Input MUX

The Input MUX consists of the switches and the Input Buffer. It selects either the input from the Analog Front End or the External, followed by a buffer. The input buffer consists of the two-stage Folded Cascaded Amplifier as shown in Figure 5. The input buffer is designed with high performance in terms of high gain and gain bandwidth such that ENOB and SNR could satisfy the resolution of sigma-delta ADC.

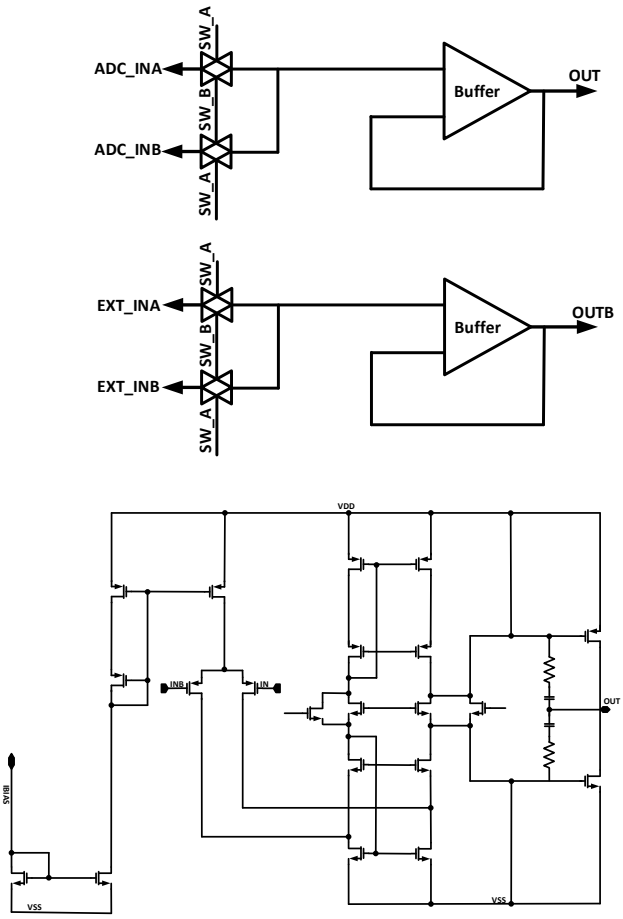

Fig. 5. Proposed schematic of Input Buffer

F. Block Diagram of Digital Decimation Filter

The Decimation Filter reduces the noise power and improves SNR performance as shown in Figure 6. To achieve this, we use a Cascaded Integrator Comb Filter (CIC) as the decimation filter, which uses adders instead of multiplication and performs averaging operation [5]. This filter is a cascade of integrator (IIR Filter) and Comb (FIR Filter). The number of the integrator and comb stages defines the order of CIC Filter.

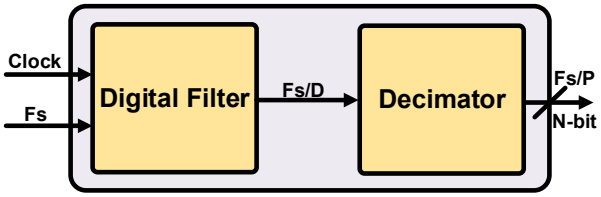

Fig. 6. Block Diagram of Digital Decimation Filter

III. Simulation Reusults

Figure 7 shows the pre-simulation results and Figure 8 shows the post-simulation results of the proposed Sigma Delta ADC at the input frequency of 1kHz. It has an ENOB of 15.2 bits and SNDR of 80.6 dB with the current consumption of 0.94mA. Figure 9 presents the Layout of the proposed ADC, and the area is 352um x 602um. Table 1 presents the summary of the proposed ADC for sensor applications.

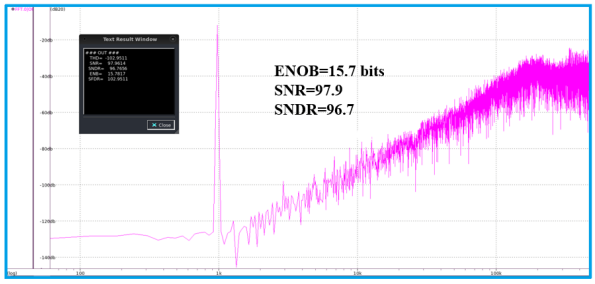

Fig. 7. Pre simulation results of Sigma Delta ADC

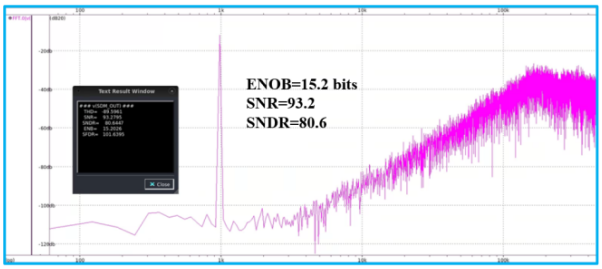

Fig. 8. Post simulation results of Sigma Delta ADC`

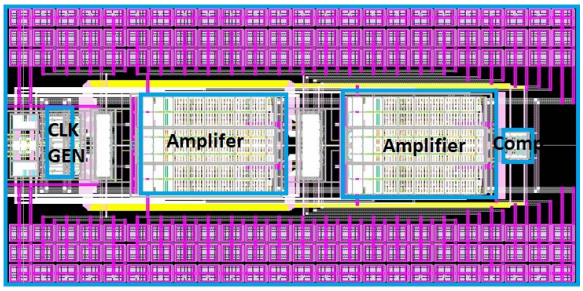

Fig. 9. Layout of Sigma Delta Modulator

IV. Conclusion

This paper presents the second order Sigma Delta ADC using 0.13µm CMOS process technology to achieve high resolution. The proposed structure has achieved an ENOB of 15.2 bits and SNDR of 80.6 dB with input frequency of 1kHz. The current consumption of the proposed structure is 0.94mA with a power supply of 1.5V. The proposed structure used for the sensor applications.

TABLE I. Performance Summary of SD ADC

Parameters	This Work
Technology	0.13µm CMOS
Architecture	Sigma Delta
Modulator Order	2
Over Sampling Ratio	512
Input Frequency (Hz)	1k
Power Supply (V)	1.5
SNDR (dB)	80.6
ENOB (bits)	15.2
Power Consumption (mA)	0.94

Acknowledge

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