Fast Locking Dual Band PLL for NB-IoT with QPSK Modulation

Jae Hyung Jung
[1]Sungkyunkwan University
[2]SKAICHIPS
[1,2]Suwon, South Korea
Republic of Korea
jbrother96@g.skku.edu

Kang Yoon Lee
[1]Sungkyunkwan University
[2]SKAICHIPS
[1,2]Suwon, South Korea
Republic of Korea
klee@skaichips.

***Abstract*— This paper represents PLL (Phase Locked Loop) for dual band communication of NB-IoT and LPWA-IoT, of which the Band width is 699MHz to 960MHz, 1710MHz to 2170MHz. The lock time of the PLL improved by combining the digital operation with analog when tracking the target frequency. In the proposed PLL architecture, many techniques are used to fasten lock time, to cover the wide range of the VCO (Voltage Controlled Oscillator) for the QPSK (Quaternary Phase Shift Keying) communication. The proposed PLL is designed with 65nm CMOS technology and covers the operating frequency range from 2624 MHz to 4471 MHz with a reference clock frequency of 30.72 MHz. The measured phase noise performance of the proposed PLL is -106.15 dBc/Hz at a VCO output frequency of 4.34 GHz at an offset frequency of 1MHz**.

Keywords—NB-IoT, Dual Band, QPSK, Phase Locked Loop

I. INTRODUCTION

Today, as technology grows faster every decade, the demand in the wireless network market for devices such as high-performance microprocessors and more efficient communication methods are required. Especially, as faster data transmission is required, one of the uprising techniques is frequency synthesis with the various modulation methods. These days, the CP (Charge Pump) PLL is used in modern communication systems. To generate wide range of LO (Local Oscillator) signal (699MHz to 960MHz, 1710MHz to 2170MHz), each VCO inductor is required for each frequency range. In this paper, we propose an advanced CP PLL design technique for broadband frequency synthesis, of which 2796MHz to 4340MHz, with a single inductor on the integrated chip for QPSK modulation. The technique of multiplexing the VCO output signals with high speed logic is used to generate each LB(Low Band) and HB(High Band) signals. To fasten the lock time of the PLL, digital operations are aided with the analog PLL to tune VC node(the input control voltage of the VCO). The operation to settle the VC node voltage by digital is called coarse tuning. After the digital operation, the analog operation, which is called fine tuning, of the PLL starts. After coarse tuning, the fine tuning operates in sequence. The PLL gets into the lock state faster than the circuit only with the analog operation.

II. PROPOSED DUAL BAND PLL ARCHITECTURE

A. Proposed PLL Top Block Diagram

Figure 1 shows the top block diagram of the proposed dual-band PLL. It consists of the 30.72MHz reference clock, PFD, the external 3rd-order loop filter, LO generator, and Divider. As the VCO should cover both unlicensed and licensed band, of which 699MHz to 960MHz, 1710MHz to 2170MHz respectively, proposed architecture of the PLL operates with additional divider to generate LO signal.

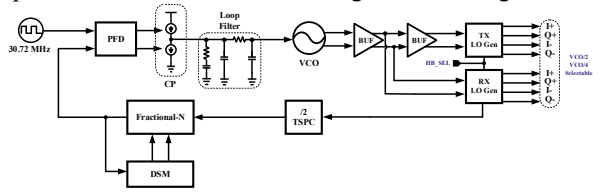

Figure 1. Top Block Diagram of the Dual Band PLL

III. BUILDING BLOCKS OF THE PROPOSED PLL

A. Dual Band PLL Top Block Diagram

The proposed Block Diagram of the designed PFD to control blind zone is shown in Figure 2. The proposed circuit has two input signals and two output signals as same as the conventional structure[1]. When fed into a phase frequency detector (PFD), the difference in phase between the two input signals, divided signal, and the reference signal, produces an output, which is up and down signals.

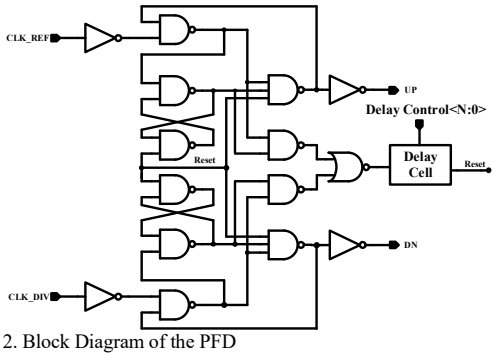

Figure 2. Block Diagram of the PFD

The conventional PFD has blind zone (or dead zone), which is the region that PFD cannot detect. The blind zone phenomenon is primarily responsible for the increase in phase noise in PFD. If the PFD is in the blind zone, it recognizes a phase error and the PLL may go into the wrong state and lock into the wrong phase. Therefore, the dead zone must be successfully controlled. To reduce the blind zone of the PFD, reset delay control is essential.

B. Charge Pump

The proposed CP (Charge Pump) block diagram is shown in Figure 3. The UGB (unity gain buffer) is used to decrease voltage step at the CP output at turning on. Due to charge sharing between the output node and both other sides of N or P switch, the voltage at the CP output shows a step when both switches are turned on. While in ideal case the output of the CP, which is the control voltage, should remain quiet. To decrease this effect, the UGB is essential. To obtain fast response and to decrease the charge sharing effect of the switch, self-Biasing cascade structure and the rail-to-rail operational amplifier is used.

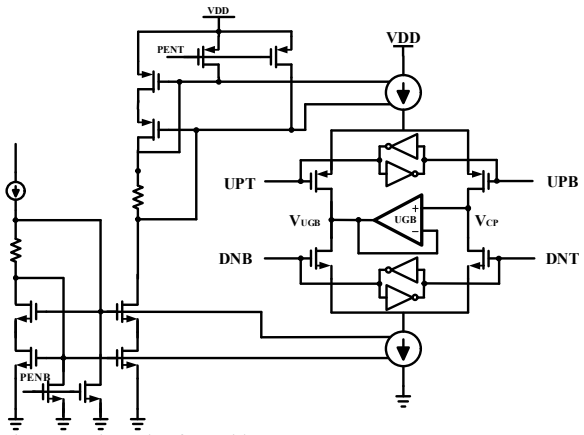

Figure 3. Schematic of CP with UGB

C. Loop Filter

Loop filters are important when designing PLLs for the operation of closed loop systems. The actual circuit of a PLL loop filter is usually very simple, but it has a big impact on the performance of the loop. The proposed loop filter is shown in Figure 4.

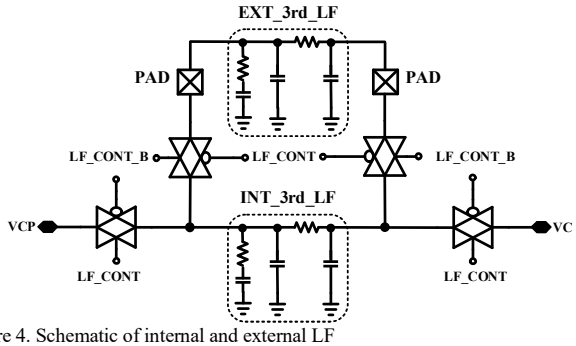

Figure 4. Schematic of internal and external LF

As the performance of the PLL loop increases, the size of the LF (Loop Filter) also increases to satisfy loop stability. A loop filter slows down the response. The narrower the loop bandwidth and the lower the filter's cut-off frequency, the slower the loop's response to changes. Conversely, if the loop requires a fast response to frequency changes, a wide loop bandwidth will be required. As the PLL demands various performance to apply different systems, the loop filter parameters should be controlled as well.

D. Voltage Controlled Oscillator

Proposed VCO (Voltage Controlled Oscillator) block diagram is shown in Figure 5. Controlling the 8 bits of the VCO capacitor bank can satisfy the target frequency. Since the target frequency is 2796MHz to 4340MHz, the VCO capacitance bank should be tuned to achieve the target frequency. Also, VCO gain should be obtained to achieve target frequency range, and to determine LF parameters to design stable and fast PLL.

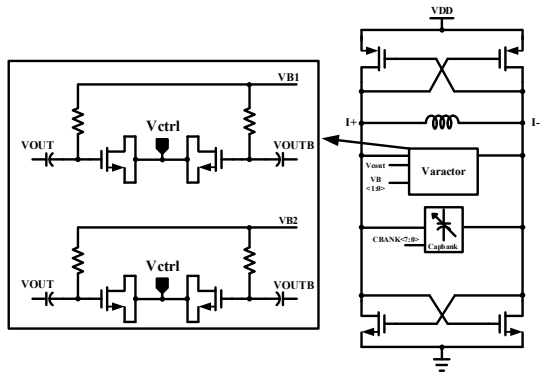

Figure 5. Schematic of VCO

E. Frequency Divider

The frequency dividers are not only used for the PLL Loop, but for generating LO signal. As mentioned in the introduction of this paper, to generate LB signal (699MHz to 960MHz), and HB signal (1710MHz to 2170MHz) separately, multiplexer is needed. By dividing by 2 and 4 for each HB and LB signal from the VCO output signal (2624MHz to 4471MHz), the multiplexer selects the dividing ratio. The block diagram for the dividers used in LO signal path is shown in Figure 6.

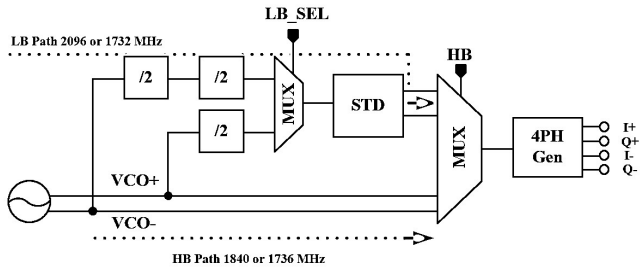

Figure 6. Block Diagram of the LO signal path

Figure 7 shows the block diagram of the feedback path, which it is composed of Fractional-N divider, DSM (Delta-

Sigma Modulator), and 13-Bit Counter. Due to the high frequency of the input signal to frequency divider, both first stage of dividers for PLL Loop and the LO signal path are designed with CMLD, which can divide up to 8GHz. Since CMLD consumes large current due to the dynamic operation and the current mode logic, TSPC is used after first dividing by 2. After dividing the VCO output signal by 4, Fractional-N divider operates with DSM to attenuate the spur from divider.

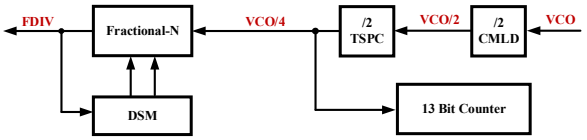

Figure 7. Block Diagram of the Feedback path of PLL

F. Digital Block for Coarse Tuning

Figure 8 shows the block diagram of the digital block in the feedback path. The counter operates with divider, LF and VCO. CNT_MASK determines the mask time of the counter to be counted. When the mask time is done, the counter adjusts the 8-bit of the cap bank of the VCO to rise or to fall. The final value gets close to the target frequency after repeating several times. This whole digital operation is called coarse tuning. Since it is done in the digital, it is faster than operating only with analog.

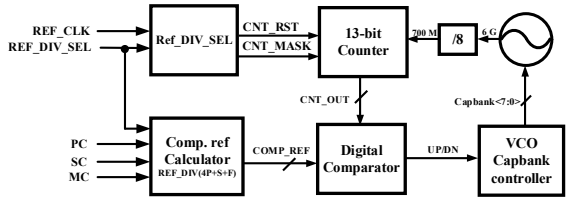

Figure 8. Digital Block for Coarse Tuning.

G. PLL Layout

The PLL was manufactured in a 65nm CMOS process. The total active area is 630x1120μm2. The layout of PLL is shown in Figure 9.

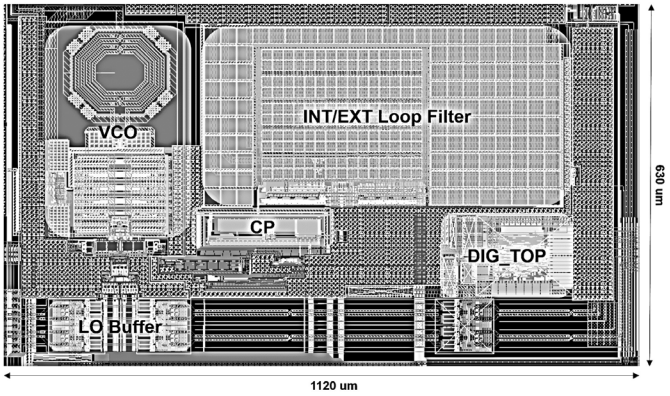

Figure 9. PLL Top Layout

IV. Simulation Results

The post layout simulation of the VCO results is shown in Figure 10 to Figure 12. The maximum and minimum frequency of the VCO, KVCO, and VCO Phase Noise are shown below. The simulation of the PLL Top results is shown in Figure 13 to 14. The lock time is 15us.

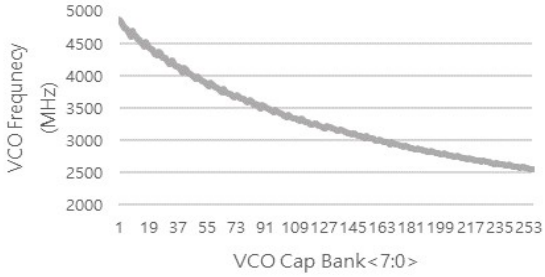

Figure 10. Simulation results of the VCO Cap bank

(a) (b)

Figure 11. VCO gain simulation result of when VCO output frequency is (a)4451MHz (b)2621MHz.

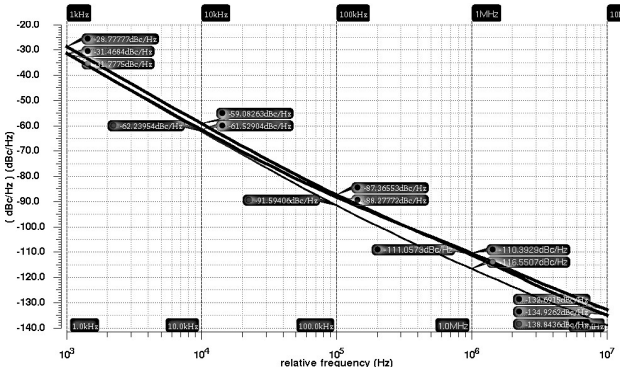

Figure 12. Simulation results of VCO Phase Noise

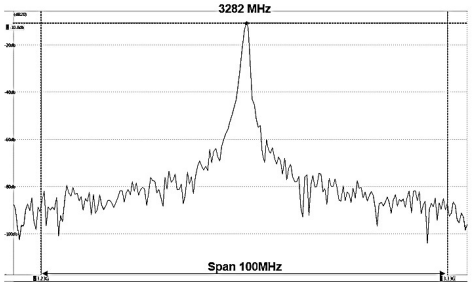

Figure 13. FFT simulation of VCO output

The post layout simulation of the VCO results is shown in Figure 10 to Figure 13. The maximum and minimum frequency of the VCO, KVCO, and VCO Phase Noise are

shown below. The simulation of the PLL Top results is shown in Figure 13 to 14. The lock time is 15us.

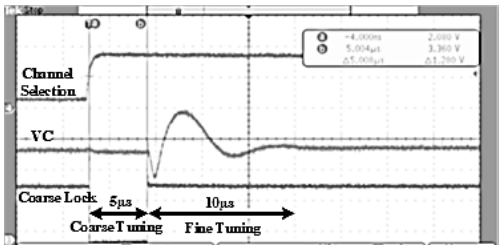

Figure 14. Transient Simulation result

V. CONCLUSION

The design of the proposed PLL was designed with a 65nm CMOS process, and the size of the entire PLL top layout including the loop filter is 630x1120μm2. The proposed PLL covers an operating frequency range of 2624 MHz to 4471 MHz with a 30.72 MHz reference clock frequency. The measured phase noise performance of the proposed PLL is -106.15dBc/Hz at 1MHz offset frequency at the VCO output frequency of 4.34GHz.

ACKNOWLEDGEMENT

This work was supported by the Technology Innovation Program (00144490, Development of Highly Efficient and Intelligent Solar Energy Harvesting System integrating 600V level GaN Device) funded By the Ministry of Trade, Industry & Energy(MOTIE, Korea)

REFERENCES

[1] Congyin Shi, Huaizhou Yang, Huiling Xiao, Junhua Liu and Huailin Liao, "A dual loop dual VCO CMOS PLL using a novel coarse tuning technique for DTV," 2008 9th International Conference on Solid-State and Integrated-Circuit Technology, Beijing, 2008, pp. 1597-1600, doi: 10.1109/ICSICT.2008.4734882.

[2] D. Biswas and G. Ahmad, "Spur Reduction in Fractional PLL using Complementary PFD-CP technique for Wireless Transceiver Design," 2022 2nd Asian Conference on Innovation in Technology (ASIANCON), Ravet, India, 2022, pp. 1-5, doi: 10.1109/ASIANCON55314.2022.9908974.

[3] J. Liang, H. Quan, D. Zhang, L. Yang and Y. Xue, "Design of a 32bit High Precision Sigma-delta Fractional Divider," 2021 IEEE 5th Information Technology,Networking,Electronic and Automation Control Conference (ITNEC), Xi'an, China, 2021, pp. 329-332, doi: 10.1109/ITNEC52019.2021.9586973.