Design and implementation of a low-area reconfigurable and synthesizable digital loop filter for ADPLL

Nabeel Ahmad
Dept. of Electrical & Computer Engineering
Sungkyunkwan University
Suwon, South Korea
nabeel8@skku.edu

Kang Yoon Lee
Dept. of Electrical & Computer Engineering
Sungkyunkwan University
Suwon, South Korea
klee@skku.edu

***Abstract*— This paper presents design and implementation of a low area and efficient Digital Loop Filter (DLF) for ADPLL application. DLF is one of the basic building blocks of an ADPLL and used to remove high frequency contents from TDC (Time to Digital Converter) output. Digital loop filter is one of the most area consuming block in ADPLL and care is required in its efficient implementation. In Analog PLL 2nd or 3rd order loop filter can be implemented using R and C passive components. The absence of passive components makes ADPLL a superior choice for low area design. In ADPLL same order filter can be implemented in z-domain. This work discusses the design and implementation of a digital filter whose coefficients can be changed adaptively hence minimizing the area due to re-using of the resources (MAC units). The coefficients are made adaptive which can be controlled using an external interface as well as a number of options (for coefficients) inside the digital block. This makes the filter convenient to use and DCO can be operated with specific region of operation. Also the filter is designed and verified in HDL using standard library cells thus making it synthesizable and can be used by any CMOS technology node. In this work the filter is implemented and simulated for 65nm technology with the area of .01mm^2.**

Keywords—ADPLL, digital loop filter, re-configurable filter, proportional-Integrator filter

I. INTRODUCTION

ADPLL stands for All Digital Phase Lock Loop and is requirement of every clock operating system that require in phase clock with minimum and time invariant jitter. It mainly consists of three blocks including a Digitally Controller Oscillator (DCO), a Time to Digital Converter (TDC) and Digital Loop Filter (DLF). A Frequency divider can be added in the feedback path to multiply the reference frequency, and get the desired frequency. These blocks are comparable to analog PLL as shown in Fig 1, along with location of digital loop filter (DLF). All the blocks can be designed in digital domain (using Verilog HDL) with synthesizable modules, hence got the name All Digital PLL.

TDC measures time difference between DCO output clock (divided by some fraction) and reference clock (Fref). This time difference is a digital output with high frequency components. Due to limited tuning range (hence LSB) of DCO, the high frequency terms should be eliminated using digital loop filter (DLF). Multiple ADPLL architectures are proposed for low area and accuracy point of view.

A DLF is proposed [1] with frequency error prediction for BBADPLL. ALM helps the system to arrive at target frequency directly and keep a reasonable gain to achieve locking. The novel DLF based BBPLL decreases the locking time to 1/24 of the traditional one, without worsening the jitter performance.

Bang-bang ADPLL eliminates the requirements of power and area hungry blocks [2] such as Time to digital converter (TDC) and ADC. The nonlinearity of BB-ADPLL makes the traditional Laplace transform used in the modelling of PLL invalid. In [2] an adjustable coefficient based loop filter is presented to control the closed loop dynamics of PLL.

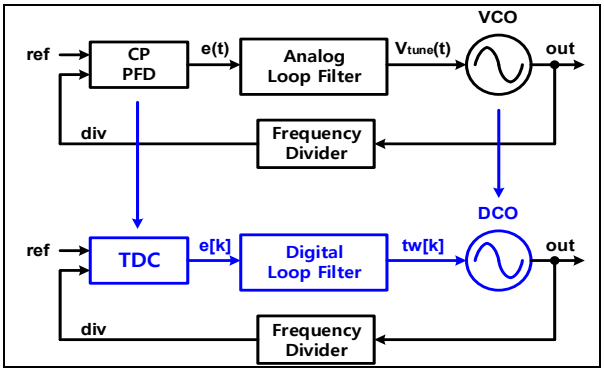

Fig.1. Analog Vs All digital PLL

An LC based oscillator can be used efficiently [3] to control the output oscillation with required frequency. Usually L is kept constant whereas capacitor bank is used to tune to the output frequency. A capacitor tank can have three major arrays including coarse, medium and fine as described in [3]. Using multiple arrays widens the tuning range and frequency resolution. This LC filter is derived by output of Loop filter to adjust at the required frequency.

Hence Loop filter has a crucial location among the ADPLL blocks and consume most of the area of an ADPLL. Proper care should be provided to design low area, with synthesizable properties for easy migration among the technology nodes. This work discusses the implementation of a loop filter for ADPLL with low area and configurability options that can be used for a variety of ADPLL structures.

II. Proposed Architecture Of Digital Loop Filter

A proportional Integrator (PI) filter can be used effectively for ADPLL, which is designed in Verilog HDL. Z-domain model of PI filter is shown in Fig 1.

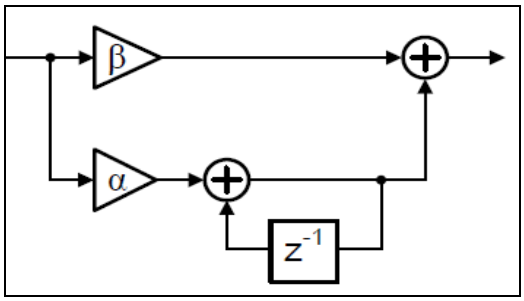

Fig 2. Z domain PI filter representation

In this work an adaptive coefficient based PI filter is designed as shown in Fig 3. Although this filter is designed for filtering output of TDC, but can be effectively used with BBPFD based design (1-bit TDC) to enhance ADPLL characteristics [4].

The TDC, DCO and the digital loop fitler values are updated at the reqference frequency f (1/T). The DCO output phase at the kth reference clock edge is

$$\theta\,[k+1] = \theta\,[k] + \omega_{\varepsilon}\,T + e[k] - n[k]$$

Where $\omega_{\varepsilon}/2\pi$ is the intial VCO frequency. The desired DCO outptu phase at the kth reference clock edge is given as

$$\theta_{des}[k+1] = \theta_{des}[k] + \omega_{des}\,T$$

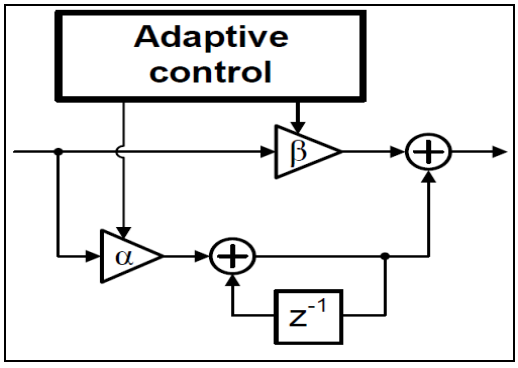

Fig 3. Adaptive coefficients PI filter

The coefficients of the Adaptive control blocks can be modified through a serial link off the chip. In this design the input data is 11 bits, and filter output the filtered 11 bits data for DCO. For our application 2nd order filter is designed by including further low filter stage with the model as shown in Fig2. The resultant PI 2nd order filter is shown in Fig3.

Also the same loop filter can be modified by adding extra unit delay in the proportional path to further suppress the DCO noise [5].

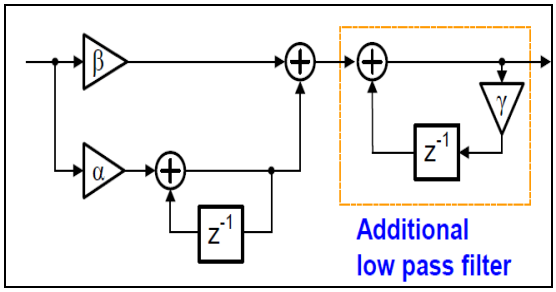

Fig. 4. 2nd Order low pass PI filter

III. IMPLEMENTATION

The proposed loop filter comprises of a proportional, Integrated, summation and delay term. They are arranged in the order as shown in Fig 5. The proposed adaptive control coefficients can be altered during operation to attain the required filtering function.

In this work the value of integrator gain (alpha) is altered to achieve the desired response. The implemented filter block diagram is as shown in the figure below;

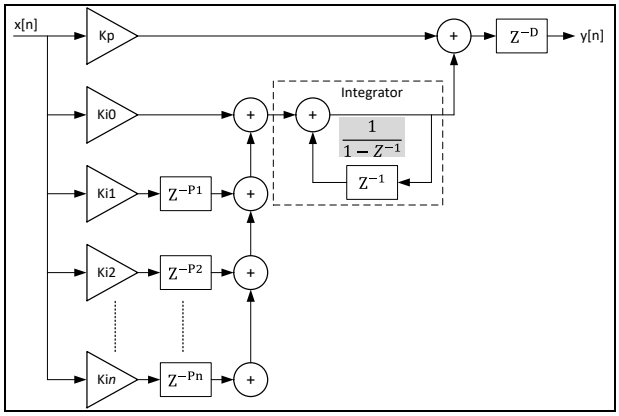

Fig 5: Loop Filter structure for ADPLL

Due to the synthesizable nature of the filter an additional stage can be added/removed to alter the loop bandwidth (increase or decrease)

The filter is implemented in VHDL, and the simplified block diagram is shown below;

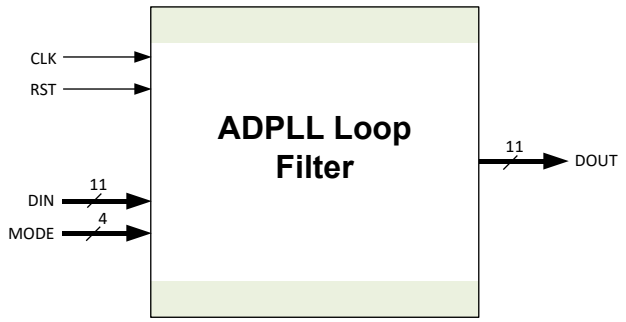

Fig 6. Loop filter block diagram

From the mode bits multiple integrator coefficients can be loaded for desired response. DIN is the input bus comprising of 11-bits from TDC whereas DOUT shows the output of the digital loop filter which are fed to the DCO.

IV. Simulation Results

Simulations are carried out in ModelSim with random and ramp input. The resultant smooth waveform can be seen as data_out_PI. A random input 11-bit in width is applied to the PI filter which mimics the TDC output showing time quantized time difference between reference and DCO output. Alpha parameters of the filter can be varied to get multiple responses from the single PI filter. Here a single mode response is shown which can be easily altered through mode bits (4-bits). In this work 10 different types of combinations can be applied for the integrator value (alpha) to achieve multiple response of the loop.

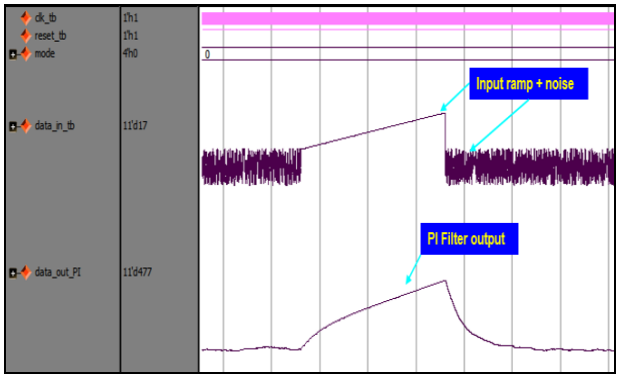

Fig 7. PI filter response for nandom+ramp input

The designed filter is synthesizable and can be used efficiently for ADPLL architecture. The functionality is verified for TSMC 65nm technology.

Acknowledgment

This research was supported by the MSIT(Ministry of Science and ICT), Korea, under the ICT Creative Consilience Program(IITP-2023-2020-0-01821) supervised by the IITP(Institute for Information & communications Technology Planning & Evaluation)"

References

[1] L. Shi, W. Gai, L. Tang and X. Xiang, "A novel digital loop filter with frequency error prediction for fast-locking bang-bang ADPLL," *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2017, pp. 1-2, doi: 10.1109/EDSSC.2017.8333239.

[2] S. Safwat, M. Ghoneima and Y. Ismail, "A design methodology for a low power bang-bang all digital PLL based on digital loop filter programmable coefficients," 2011 International Conference on Energy Aware Computing, 2011, pp. 1-4, doi: 10.1109/ICEAC.2011.6136676.

[3] J. Xiang, L. Ma, L. Zhu and H. Min, "Design of a wideband digitally controlled oscillator," *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2014, pp. 1-3, doi: 10.1109/ICSICT.2014.7021606.

[4] S. Jang, S. Kim, S. -H. Chu, G. -S. Jeong, Y. Kim and D. -K. Jeong, "An Optimum Loop Gain Tracking All-Digital PLL Using Autocorrelation of Bang–Bang Phase-Frequency Detection," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 9, pp. 836-840, Sept. 2015, doi: 10.1109/TCSII.2015.2435691.

[5] W. Namgoong, "A Modified Proportional–Integral Loop Filter to Suppress DCO Noise in Digital PLL," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 8, pp. 974-978, Aug. 2018, doi: 10.1109/TCSII.2018.2794821