

# Differential Packet Level Index Modulation for Low Power Wide Area System

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**Abstract**—The purpose of this study is to gain an information added besides the transmitted data obtained by packet modulation. The Packet-Level Index Modulation (PLIM) method is proposed to obtaining the additional data bits because the Low Power Wide Area system (LPWA system) is forced to limit a transmission period regulated by a Duty Cycle (DC). The PLIM needs to synchronize the time slot between a transmitter and a receiver due to a clock drift caused by a less-accurate oscillator of sensor nodes. This paper studies on a differential-PLIM method (D-PLIM) to reduce the overhead spent for the time synchronization. D-PLIM performs an index data detection by basing a previous packet index without the time slot synchronization. Therefore the D-PLIM is less affected by the clock drift than by the normal PLIM. This paper shows the simulation results for evaluating the effectiveness of D-PLIM.

**Index Terms**—Low Power Wide Area, Packet-Level Index Modulation (PLIM), Differential-PLIM (D-PLIM), clock drift

## I. INTRODUCTION

Recently, the Internet of Things (IoT) is focused as one technology to realize our more comfortable life in future. IoT systems collect information from multiple sensors, for example a temperature meter, a humidity meter, and so on. The collected-various data about the environment of each sensor are used for improving the bad situation. In IoT systems, a capability to capture immediate situations increases by collecting its multiple data from many sensors. Therefore, the IoT system consists of wireless sensor network.

In general, Low Power Wide Area (LPWA) is embraced by IoT systems because the IoT sensors are placed over a wide range and are powered by a limited electricity capacity. In many cases, the sensors have to economize the power to obtain a longer life because each sensor is driven by a battery without indefinitely-supplied powers. In addition, LPWA systems are forced to restrict a transmission period by a regulation called duty cycle (DC).

The DC defines an available transmission period per a certain time of wireless nodes. According to a system, the DC of its nodes describes that of every channel or the sum of that over all channels. In a general case, the DC is set to 1 %. The DC condition leads the nodes to share limited wireless resources as evenly as possible when the number of IoT nodes is large. Therefore, communication rates of the IoT systems are a far lower than that of other wireless systems such as a wireless LAN, because the node has to communicate with

others within the limited available time. In IoT systems, nodes can achieve a certain task of the system by packetizing a few bits in one packet.

However, it is obvious that a system flexibility is increased when the number of communication bits increases. Under the condition mentioned above, there is a proposed method for LPWA system to increase the transmission bits per one packet. The proposed method is called packet-level index modulation (PLIM) [1]. The PLIM method can obtain additional bits by utilizing indexes of a time slot dimension and a channel dimension separately from the data to be transmitted by packets. The amount of the additional data is decided by the number of indexes because symbols are assigned to those index numbers.

A detection performance of PLIM is decided by an accuracy of an oscillator with which each sensor is equipped. The reason is that a time slot interval which consists of a series of the time index cannot be correctly detected when the sensor's clock is not with accuracy. Such jitter of clocks differs from node to node because node's oscillators have an individual difference. Therefore the clock is ahead or behind depending on the node. In this case, the detection error of PLIM is wreaked by the clock drift caused by the low-accuracy oscillator. The clock drift cannot be elided because the nodes in IoT systems are produced cheaply in large numbers [2]. In order to decrease its influence, IoT systems with PLIM need to synchronize the time between a transmitter and a receiver to detect the time slot index number.

IoT systems consist of a lot of sensors, and its cost is decided by considering all sensors' cost. Therefore, to equip the sensors with GPS device to know the absolute time cannot be expected because it is better that prices per a sensor is low. The sensors do not have an ability to turn the absolute time by one self. Thus, at the beginning of PLIM, the receiver such as a gateway has to know a relative time of every sensor. The shifted amount of the sensor's clock is accumulated depending on the elapsed time. Moreover, the amount of the clock drift of each node slightly changes on a moment-to-moment basis.

Then, the IoT system with PLIM needs the time synchronization to decrease the PLIM detection error rate. The time synchronization is generally performed by transmitting a control signal from a gateway to sensor nodes. The sensor's clock gradually loses time with the increase in the elapsed

time from the latest synchronized time. Therefore the sensors have to inform a demodulator of PLIM such as the gateway as to the sensor's time regularly. In a real environment, the control signals for the time synchronization are transmitted at a regular interval in addition to the packet transmission. In this case, it is obvious that an extra resources need to transmit the control signals for the time synchronization performed between a transmitter and a receiver. This cost is unavailable to be excluded in the operation of the general PLIM.

In this paper, in order to decrease the influence of the clock drift of the sensor in PLIM, a differential-PLIM (D-PLIM) is proposed. D-PLIM method uses a detected time of a previous transmitted packet as a reference value for PLIM transmission data. Because the gateway can detect the additional data by referring to the previous detected time, D-PLIM does not need to synchronize the time by a control signal. However, when the previous packet cannot be demodulated, the gateway loses not only the previous received PLIM data but also PLIM data transmitted by the last packet.

This paper introduces the D-PLIM method and shows the performances by the numerical simulation. We discuss the effectiveness of the D-PLIM by using these simulation results.

## II. PREVIOUS WORK

### A. Packet-Level Index Modulation

The packet level index modulation (PLIM) has been proposed by the literature [1]. PLIM uses a slot index number in a time dimension and a channel index number in a frequency dimension to add a few data except for payload included in transmitted packets. To increase such utilizable bits is useful for IoT systems, because the amount of data transmitted by one packet is not very much in LPWA systems.

In IoT systems, a wireless sensor node which is a transmitter transmits its own measured data to a gateway. The network consists of a huge number of sensor nodes and the gateway. Communications in IoT are performed with sharing the finite frequency resource. Therefore, the transmission period per one node is regulated by a duty cycle (DC), which is set to 1 % generally.

In PLIM, the DC is satisfied, because there are unused time slots by allocating a symbol to each time slot index number. A frame is defined as a period which consists of some slots. In the most basic case, the number of slots being a power of two is used. One packet is transmitted at one of the slots within one frame as shown in Fig. 1. Then, the remaining slots within its frame are not used. That is to say, the sensor nodes can keep the DC condition when the packet length and the frame length are set adequately, because the DC is just the ratio of transmission period to a certain operation time.

## III. DIFFERENTIAL PLIM

The PLIM scheme can increase the amount of data to be transmitted in addition to the transmission information by conventional packet communication by using the transmission channel and timing of packets without changing the existing packet modulation scheme of LPWA. However, in order to

Fig. 1. A frame and a slot for PLIM.

accurately recover the index used by PLIM at the receiver, it is necessary for the transmitter and receiver to share in advance the start time information of the frame in which a packet is transmitted. The frame start time information (time synchronization) must be repeated after a certain period of time depending on the clock accuracy of the transmitter terminal, and periodic time synchronization can suppress demodulation errors in transmission information by PLIM. Interrupting packets with periodic frame synchronization information is costly when implementing a PLIM scheme, so a method that does not require time synchronization is needed.

Although the slot length design using the margin of slots can reduce the number of time synchronizations [3], it cannot eliminate time synchronization between transmitters and receivers because time deviations accumulate over the operation time of the system in the long term. Furthermore, the slot length margin should be set to be as short as possible, considering the efficiency of the PLIM system. However, a short slot-length margin increases the effect of clock drift, so the relationship between these is a trade-off.

Differential packet-index modulation (D-PLIM) is a method that can reduce the frame synchronization between a transmitter and receiver, which is a cost of PLIM. This section describes the procedure of the D-PLIM scheme. D-PLIM differs from PLIM in that it uses the indexes of the previous packet to determine the indexes of a packet instead of the frame synchronization between the transmitter and receiver, while PLIM is the underlying technology.

The modulation and demodulation procedures of D-PLIM are shown below.

- 1) For the first packet to be transmitted, a random or predefined channel index,  $K_0$ , and time slot index,  $Q_0$ , are selected. The number of channel indexes is  $K$  and the number of time slot indexes is  $Q$ , which is the number of slots of one frame.
- 2) The selected indexes are used to transmit packets. Up to this point, it is the same as the conventional LPWA method without PLIM.
- 3) If there is no packet to be transmitted, it waits until a transmission packet is generated, and then moves to the following procedure for transmission in the next frame when transmission information is generated.
- 4) As before, packets are generated using the LPWA modulation scheme.
- 5) The appropriate indexes are selected according to the transmission information of the PLIM to be transmitted

Fig. 2. D-PLIM at a transmitter  
(The channel index  $K = 4$ , the time index  $Q = 4$ )

in the next frame. Here,  $D_i^H$  and  $D_i^L$  denote the upper and lower bits of the transmission information by PLIM, respectively. The channel index,  $k_i$ , and time index,  $q_i$ , of the  $i$ th packet to be transmitted are calculated using the following conversion equations.

$$k_i = (D_i^H + k_{i-1}) \bmod K \quad (1)$$

$$q_i = (D_i^L + q_{i-1}) \bmod Q \quad (2)$$

This process means that information is placed on the difference from the indexes of the previous packet.

- 6) The  $i$ th packet is transmitted in a frame using channel  $k_i$  and time slot  $q_i$  calculated from the above equations (1) and (2).
- 7) If there is a packet to be transmitted in the next frame, the procedure is repeated from 4. If there is no packet to be transmitted, the procedure is repeated from 5 in its frame at when the next packet is generated.

As described above, the exchange of information about the frame start time, which was necessary in the PLIM scheme, is not performed in the D-PLIM. However, the indexes of the first packet to be transmitted cannot be assigned PLIM transmission information. Therefore, the indexes of the first packet to be transmitted is selected randomly or predetermined indexes are used.

Figure 2 shows an example of sending the  $i$ th packet and the  $i + 1$ th packet at the  $m$ th terminal. The indexes of the packet sent in the  $i$ th frame in Figure 2 are assumed to be the randomly determined indexes  $(k_i, q_i) = (3, 2)$ . Here, it is assumed that the channel and time slot indexes are 00, 01, 10, and 11, respectively, from the smallest to the largest, and that the PLIM transmission information is  $D_{i+1} = 0110$ . The next indexes are obtained from equations (1) and (2), respectively, that is  $(k_{i+1}, q_{i+1}) = (0, 0)$ .

Next, the demodulation procedure at the receiver is shown.

- 1) The terminal number and packet number in the header of the received packet are demodulated and stored in the database together with the index of the receiving channel and the reception time. Assuming that the packet number is  $i$ , the received channel index and received time are represented by  $k_i$  and  $t_i$ , respectively.

Fig. 3. D-PLIM at a receiver  
(The difference between channel indexes of packet number 0 and 1,  $K + (k_i - k_{i-1}) = 1$ , the difference of reception times,  $t_i - t_{i-1} = 2$ )

- 2) If the  $i - 1$ th packet is received, the PLIM transmission information can be demodulated using the following equations.

$$\widetilde{D}_i^H = (k_i - k_{i-1}) \bmod K \quad (3)$$

$$\widetilde{D}_i^L = \left( \frac{t_i - t_{i-1}}{T_{\text{slot}}} \right) \bmod Q \quad (4)$$

where  $\widetilde{D}_i^H$  and  $\widetilde{D}_i^L$  represent the upper and lower bits of the PLIM transmission information, respectively.  $T_{\text{slot}}$  represents the slot length, which is the received time divided by the slot length and rounded to the nearest integer. In the equation (3), when  $k_i - k_{i-1}$  is negative,  $K$  is added and then bit shifted. If the  $i - 1$ th packet has not been received, the PLIM transmission information cannot be demodulated, so it waits until the next packet is received.

- 3) Thereafter, the procedure is repeated from 1.

As shown in Figure 3, the D-PLIM scheme can demodulate PLIM transmission information by being based on the difference between the indexes of the current packet and the previous packet, even if the start time of the frame is not known at the receiver. However, if packets with consecutive packet numbers cannot be received, PLIM transmission information cannot be demodulated. In addition, the first packet or the first packet after packet loss cannot demodulate the PLIM index because one previous packet has not been received. Therefore, a disadvantage of the D-PLIM scheme is that the PLIM demodulation rate degrades in an environment where packet loss occurs frequently. On the other hand, the differential index modulation limits the effect of clock drift caused by inexpensive oscillators at the transmitter. This is because the clock drift is affected only between the reception of the previous packet and the reception of the next packet.

#### IV. SIMULATION EVALUATION

In this paper, the tolerance of the proposed D-PLIM method to time deviation is evaluated by simulation.

##### A. Simulation Environment

The simulation system is assuming that one node and one gateway exist, in order to avoid the influence of interference. Thus, all of the transmitted packets of the sensor node are received without failure. In this paper, only the effect of time deviation is evaluated. Therefore, the effect of frequency

Fig. 4. Index detection in the conventional PLIM method.

TABLE I  
SIMULATION PARAMETERS

Number of Channel	2
Number of time slots per one frame	$2^5$
Slot length	Same as the packet length
Margin included in the slot	0
Number of sensor node	1
Number of attempts	1,000

dimension is ignored. The number of indexes and the frame length are fixed. One trial is a period of time until the transmission of the specified number of packets are completed. The simulation results are averaged over 1,000 trials.

In the simulation, the clock drift of the sensor node is generated as a constant percentage of the elapsed time. In a real environment, time deviations are assumed to be averaged at a certain value and fluctuate with a Gaussian distribution [3]. For simplicity, we assume that the time deviation caused by the clock drift is a constant value that accumulates in a positive direction with elapsed time.

In this paper, the conventional PLIM method and the proposed D-PLIM are compared. In the conventional PLIM, time synchronization is performed only by the first transmitted packet. When a received packet is detected spanning two slots, the one with the longer packet fraction is used as the detection time index number, as shown in Fig. 4.

#### B. Simulation Results

Fig. 5 shows the results when the number of transmission packets is set to 5, 10, 30, respectively. The horizontal axis shows the ratio of the time deviation to the slot length, assuming an environment in which the time deviation is accumulated and received according to the simulation elapsed time in units of the slot length.

As can be seen in Fig. 5, the PLIM symbol detection error rate increases with the conventional PLIM when the number of transmitted packets is large. This is because the effect of accumulated clock drift increase throughout one execution due to the fact that only one time synchronization is performed in this simulation. For example that the ratio of clock drift to slot length is 0.4%, if the PLIM error rate is to be kept within 10%, the time synchronization has to be performed once every five frames by using some control signal. Moreover, in the case that its ratio is 0.2%, if the condition is same, the time synchronization has to be performed once every 10 frames.

On the other hand, when the proposed D-PLIM is used, the error rate is low regardless of the number of transmitted packets, because only the effect of the clock drift between two packets received in sequence depends on the PLIM symbol error rate. However, when the ratio of the clock drift to the slot

Fig. 5. PLIM symbol detection error rate for clock drift.

length is greater, the PLIM detection error performance with the D-PLIM is also affected by the clock drift between two packets received in sequence. However, in an actual system, it is unlikely that a poor oscillator with a clock drift of more than 1% to slot length would be installed in a wireless sensor node, so there is no operational problems in D-PLIM.

#### V. CONCLUSION

In this paper, based on the PLIM method, which is expected to be applied to LPWA systems, the Differential PLIM (D-PLIM) method is proposed. This paper shows the simulation evaluation of the effect of the proposed D-PLIM method on clock drift. A periodic time synchronization is necessary when PLIM is used in LPWA, because it is expected that inexpensive wireless sensor nodes will be used for communication. Whereas the proposed D-PLIM does not require the time synchronization, in addition to the transmission of information in packets, an increases in the number of transmitted bits can be expected by using index numbers to transmit additional bits as with the conventional PLIM. Simulation result of PLIM symbol detection error rate confirms that the proposed D-PLIM is more tolerant of clock drift than the conventional PLIM.

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