Design of DC-DC Boost Converter With Digital Pulse Width Modulation for Transducer

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Abstract— In this paper, we design a DC-DC Boost Converter for driving transducers. To maximize power, we study the circuit techniques required for HV Pulser using digital feedback techniques. Boost DC-DC converters are expected to benefit in area and cost by implementing low-power, low-area circuits using digital feedback loop. This paper designed the required circuit using the 0.13um process. The designed Boost DC-DC converter converts 3.7V input to 12V output voltage. Provides up to 89% efficiency when supplying 100mA.

Keywords—Boost DC-DC Converter, DPWM, Bootstrap, Hybrid Core, Window ADC, Digital Compensator

I. INTRODUCTION

As markets for smartphones, tablet PCs, and wearable devices continue to develop with the recent development of miniaturized devices, interest in the Internet of Things (IoT) is increasing. With the miniaturization of products, portability and convenience are developed, and performance is continuously added to meet the needs of various consumers. The same is true of ultrasonic transducers. Recently, ultrasound markets require technology that implements low power and miniaturization as well as high resolution. But for high resolution, channels need to be increased. As a result, area and power consumption are increasing proportionally. In this paper, we design Boost DC-DC Converter to drive HV Pulser required for transducers. Switching type DC-DC converters have the advantage of being able to generate high-efficiency properties by increasing or decreasing output with input voltage. However, DC-DC converters need compensation to ensure the proper stability of closed-loop transfer capabilities for feedback. At this time, external device resistance and capacitors used for compensation have problems with increasing cost and area.

To address this problem, we want to design a digital PWM(DPWM) DC-DC converter. DPWM DC-DC converters reduce device costs and pad area by not using external devices. We Propose a DPWM core with low power and high linearity to provide high efficiency. By reducing sensitivity to the external environment such as process, voltage, and temperature(PVT), miniaturization devices exposed to various external environments can be operated independently.

II. ARCHITECTURE OF BOOST DC-DC CONVERTER

A. Boost DC-DC Converter

Recently, many circuits have changed from Analog to Digital. The benefits of Digital are not only low power storage, but also less impact from PVT Variation (Process, Voltage, Temperature) and load than Analog. Figure 1 shows the top block diagram. It consists of Window ADC, Digital Compensator, Hybrid Core, Dead Time Generator, CLK Generator, Driver and Core. The input voltage is 3.7V, the output voltage is 12V, the inductor value is 8uH, the load resistance is 120 ohms, and the load current flows approximately 100mA. A digital feedback loop was used for low power and low area. DPWM with a duty frequency of 2MHz was created using the Window ADC, Digital Compensator, and Hybrid Core. Dead Time Generator was performed to prevent both Power MOSFET from turning on. The output voltage is then generated by the on/off operation of the power MOSFET through the Gate Driver.
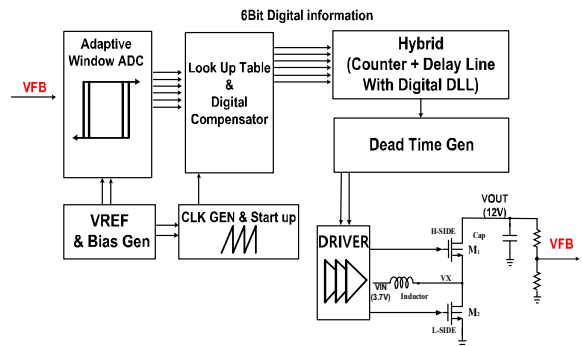

Fig. 1. Block Diagram of Boost DC-DC Converter

B. Power MOSFET and Gate Driver

As the Power MOSFET grows in size, the On-Resistance decreases. However, as the Power MOSFET grows in size, the Parasitic Capacitor component increases and the switching loss increases. In addition, the appropriate Power MOSFET should be selected, considering the share of Power MOSFET in the entire layout. In this paper, Power MOSFET consists of LDMOS to extract optimized efficiency. LDMOS has a VGS

of 5V. Therefore, since the High Side MOSFET is configured as NMOS, a VGS voltage is required for the Power MOSFET to perform switching operations. Figure 2 Shows high side Gate Driver. When using N-type Power MOSFET, these Level Shifter and Inverter Driver are combined. Using the bootstrap method, the high side output is as high as the VBOOT node than the VX node. The VBOOT voltage applies 5V through the Schottky diode, giving it a VGS 5V capable of operating the high side MOSFET.
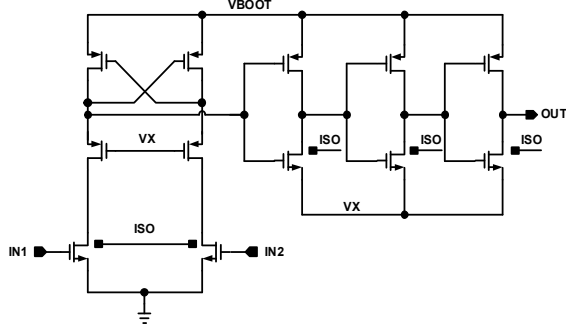

Fig. 2. Schematic of High Side Gate Driver

C. Adaptive Window ADC

Figure 3 shows the Adaptive Window ADC circuit diagram. Adaptive Window ADC receives feedback from the 1.13 V voltage generated by the BGR and the output of the Boost converter to convert the Analog signal to Digital. Compare Boost output VFB signals to Window ADC reference voltages VREF_H and VREF_L and show output signals of 0,1,-1. It uses a VFB signal and two comparators to output a 2 bits signal, which is 10, 00 and 01. At this time, the output ripple and regulation speed are determined by the Resolution of the Window ADC, so the appropriate resolution should be selected. For conventional Window ADCs, high output ripples occur, and Adaptive methods have been used to compensate for this. If the output of VREF_H is in the high state, the next comparator will be output via 2x1 Mux so that it can be compared at a voltage of VREF_AH lower than VREF_H. VREF_L is equally configured to have VREF_L selected as VREF_AL and output. This allows the output Ripple of the DC-DC Converter to be lowered from 50 mV to 20 mV. Shift register is configured for Look Up Table matching.
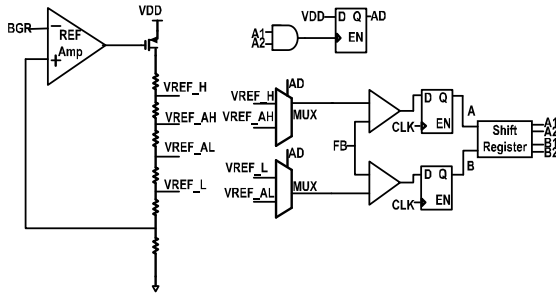

Fig. 3. Block Diagram of Adaptive Window ADC

D. Digital Compensator

Figure 4 shows the Digital Compensator circuit diagram. A total of 6 bits of Window ADC output and Shift Resister output are received and matched to the set Look Up Table. A total of 27 occurrences occurred, but the logic was constructed for the remaining 11 except those that could never occur. The Up, Down, and Stay signals from the Look Up Table enter the input at the 5-bit counter. The 5 Bit counter produces a control bit that increases and decreases in signal growth or remains constant. Only the bottom 3 bits are configured to enter the Hybrid Core. It is configured to increase the number of bits through external SPIs if high resolution is desired.
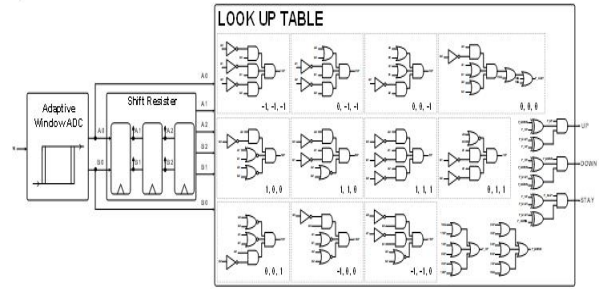

Fig. 4. Block Diagram of Digital Compensator

E. Hybrid Core

Figure 5 shows the Hybrid Core block diagram. It is an all-digital Delay-Locked Loop(DLL) structure used by the DPWM Hybrid core delay-line. The reason for using DLLs is that it cannot generate an exact duty if only the number of unit delays is matched, so the delay is fixed using DLLs. In the case of fine delay, several delay-lines were created again in the unit delay cell and the number of delay-lines was set using the up-down counter. We select the number of Unit Delay Cells to course them, and precisely implement Duty by adjusting the Fine Delay of each unit delay cell.
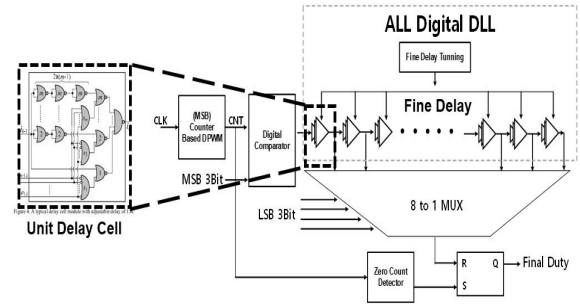

Fig. 5. Block Diagram of Hybrid Core

III. EXPERIMENTAL RESULTS

Figure 6 shows the top layout of the Boost DC-DC Converter. The top layout is designed in the TSMC 130 nm CMOS process. The area of the Boost converter is 2100 μm × 570 μm.
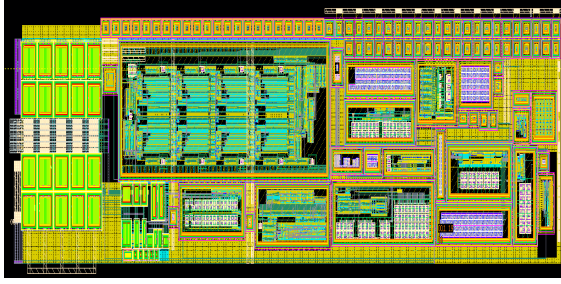
Fig. 6.   Layout Boost DC-DC Converter

Simulation results were experimented in three categories. It was first implemented by combining Windows ADC and digital compensator. Next, we added Hybrid core to check delay cell. Finally, we check Boost voltage values and efficiency and current.

A. Window ADC and Digital Compensator Simulation

The feedback voltage of the triangular wave is applied to verify the Window ADC output, and the resulting digital signal is 6 bits. When the FB voltage is less than VREF_AL (1.12V), the UP signal is generated to raise the output voltage, and when the FB voltage is greater than VREF_AH (1.14V), the DOWN signal is generated to decrease the output voltage. If an FB voltage exists between VREF_AL and VREF_AH, it maintains the output voltage through the STAY signal.
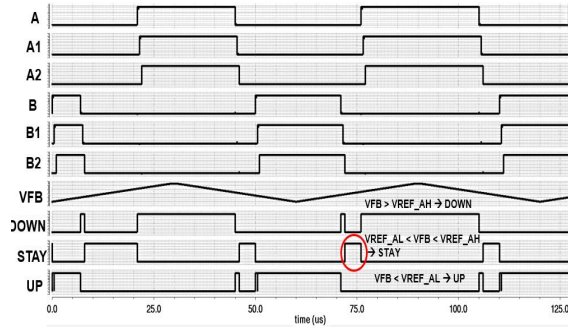

Fig. 7.   Simulation Result of Window ADC and Digital Compensator

Figure 7 is simulation result. Depending on the feedback voltage, the digital signals are well generated, and the output voltage ripple is approximately 20 mV.

B. Hybrid Core Simulation

Figure 8 is simulation result of Hybrid Core. When the signal from the compensator is set to STAY, it becomes DUTY1. DUTY1 is the on/off ratio of power MOSFET, rising from 3.7V to 12V. If the vout exceeds a certain range and the FB value increases, a DOWN signal is generated by the compensator as shown in Figure 8, resulting in as many duty signals as DUTY2.
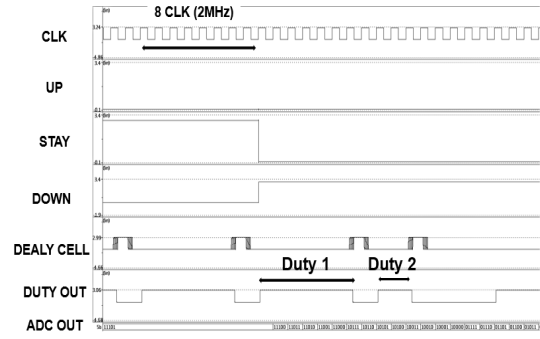

Fig. 8.   Simulation Result of Hybrid Core

C. Boost DC-DC Converter Simulation

Figure 9 shows Boost Converter Simulation. The operating frequency is 2 MHz, with a Boost Out voltage of 12.07 V and an input voltage of 3.7 V. The load current flows approximately 100 mA and the output voltage is regulated.
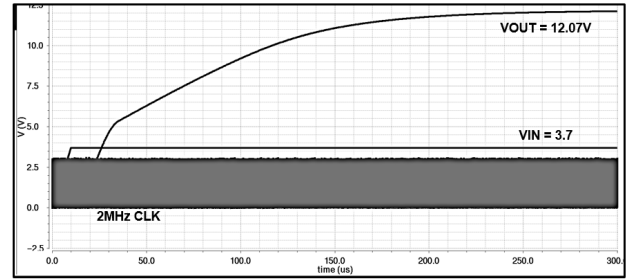

Fig. 9.   Boost Converter Simulation

IV. CONCLUSION

TABLE I.   PERFORMANCE SUMMARY

performance	
Parameter	*This work*
Process(nm)	130
Supply Voltage(V)	3
Input Voltage(V)	3.7V
Output Voltage(V)	12V
Efficiency(%)	89%
Current consumption(mA)	1.2

Table 1 shows Performance Summary. This design allows us to design DC-DCs with high power efficiency and good regulation performance. The importance of low power and low area required for Transducer is increasing. In this situation, the above study is expected to be good for high value and especially for situations that require low-area low power such as IoT.

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