12-Bit 5 MS/s SAR ADC with Hybrid Type DAC for BLE Applications

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***Abstract*—** This paper presents a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) designed for a Bluetooth Low Energy (BLE) application. The objective of this work is to reduce the number of capacitors in the Capacitor Digital to Analog Converter (CDAC). To achieve this, a hybrid type DAC has been applied where 8 Most Significant Bits (MSB)s are decided through capacitive DAC and 4 Least Significant Bits (LSB)s are decided in a Resistor DAC (RDAC). The conversion speed for this design reaches up to 6 MS/s. The prototype ADC is designed in a 90 nm complementary metal-oxide semiconductor (CMOS) process. The analog and digital supply voltage range for this design are 2.7–5.5 V and 1.1–1.3 V respectively. For 6 MS/s conversion rate, this ADC achieves up to 11.8 and 11.2 effective number of bits (ENOBs), for maximum and minimum supply voltages respectively. The current consumption from a 5 V supply voltage is 980 µA and the Figure of Merit (FOM) is 229 fJ/Conv.step.

Keywords—ADC; DAC; SAR; Hybrid DAC

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are widely used in almost all Application-Specific Integrated Circuit (ASIC) systems as the interfaces between the analog and the digital parts. Different ADC topologies are applied for different applications. Due to the recent design improvements in Successive Approximation Register (SAR) ADCs, such as conversion rate increment, increased resolution and reduced power consumption, these structures have become more popular, and they are widely used in circuit design. Capacitor arrays are usually applied as the Digital-to-Analog Converter (DAC) sub-blocks in these structures. Nevertheless, as the resolution of these structures increases, the number of the capacitors in the Capacitor DAC (CDAC) also increases enormously, which makes the structure bulky [1,3]. In addition, the mismatch between the largest and smallest capacitances in the CDAC degrades the performance of these structures [4–5]. To solve the mismatch issue in the CDAC, the unit capacitors sizes should be increased. Nevertheless, this approach increases the area of these structures.

The contribution of this work is to reduce the number of capacitors in the CDAC where the ratio of the largest and smallest capacitance can be also reduced. To reduce the area and the number of the capacitors in the capacitor array, and to reduce the mismatch problems of the CDACs, a hybrid-type DAC [6–8] is applied, in which the 8 Most Significant Bits (MSB) are determined in the CDAC, and the 4 Least Significant Bits (LSB) are decided through a Resistor DAC (RDAC) reference voltage applied to the LSB capacitor of the CDAC. This work presents a 12-bit SAR ADC that is designed to be applied in a Bluetooth Low Energy (BLE) application.

The remainder of this paper is organized as follows. Section II discusses the architecture of the proposed SAR ADC. Section III presents the layout and experimental results of this structure. Finally, section IV concludes the paper.

II. ARCHITECHTURE OF THE PROPOSED SAR ADC

Fig. 1, presents the block diagram of the proposed SAR ADC to be applied for BLE applications. This structure applies 5 V for analog and 1.2 V for digital parts. Nevertheless, the analog supply voltage can vary from 2.7 V up to 5.5 V. This variation for digital supply is 1.1–1.3 V. The different supply voltages for analog and digital require Up and Down Level Shifters (ULS & DLS) between these blocks to increase or decrease the level of the signals in the structure. The analog parts apply 5 V transistors and digital circuits use 1.2 V devices.

The designed ADC supports both single-ended and differential input signals. For single-ended mode, 24 input signals can be selected via input MUX. For the symmetry purposes of the differential mode, in negative signal path also there should be a dummy MUX. This structure supports rail-to-rail input voltage ranges and applies a 5 V reference voltage which is a Process, Voltage, and Temperature (PVT) independent DC voltage (REFT5P0V in Fig. 1). REFB in Fig. 1, is a 0 V bottom reference voltage. The applied dynamic comparator of this design is similar to ref. [5].

As mentioned before, the contribution of this work is to reduce the number of capacitors in the CDAC where the ratio of the largest to smallest capacitance can be also reduced. The structure of the applied hybrid type DAC is presented in Fig. 2. 8 MSBs are decided by switching the capacitors in the CDAC from MSB to LSB. The switching process follows VCM-based straightforward scheme which can be found in [4-5]. This switching scheme reduces the switching energy compared to conventional one. 4 LSBs are decided in the RDAC where the generated reference voltage is applied to the LSB capacitor of the CDAC.

For the proposed hybrid type DAC, including CDAC and RDAC, total number of capacitors in CDAC is 128C and total

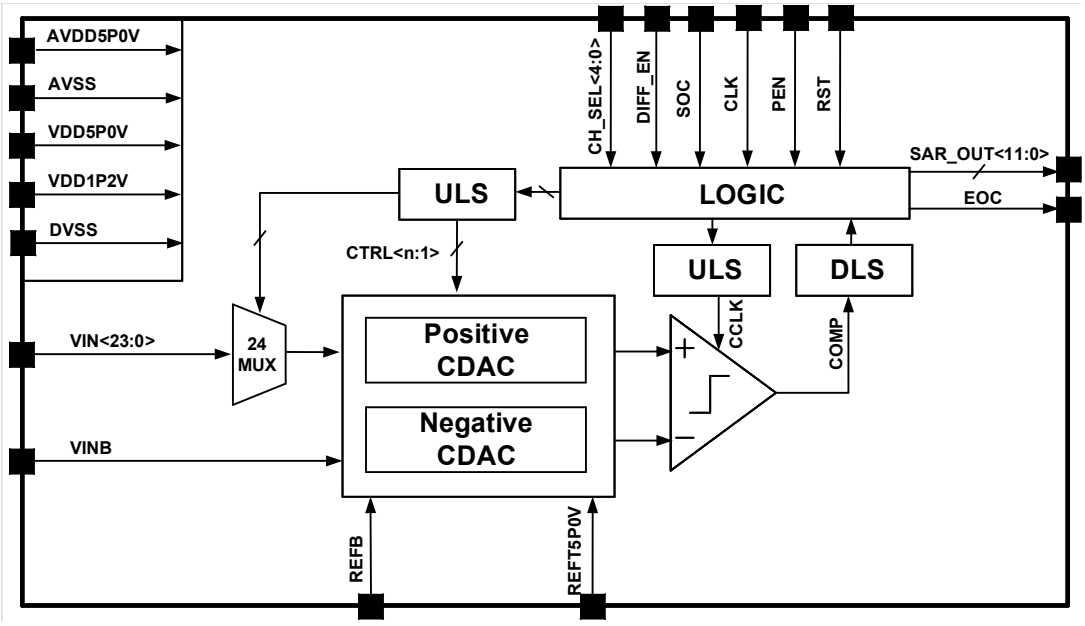


Fig. 1. Block diagram of the proposed SAR ADC

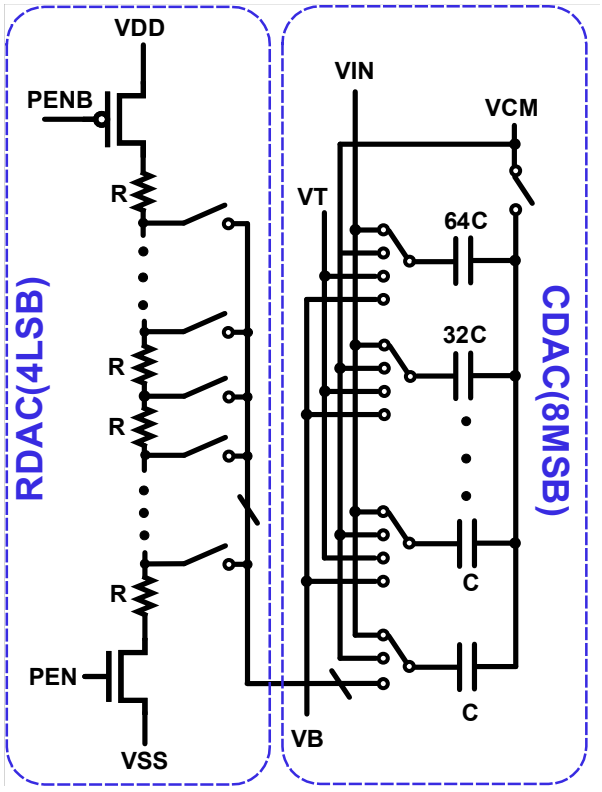


Fig. 2. Structure of the applied hybrid type DAC

number of resistors in the RDAC is 32R. This value for a 12-bit VCM-based straightforward switching CDAC structure is 2048C. This means 16 times reduction in the total number of capacitances (at the cost of additional 32 resistors in the RDAC which is negligible). Furthermore, the ratio of the MSB to LSB capacitors is 64 for hybrid CDAC-RDAC and 1024 for only CDAC structures. Therefore, the mismatch in CDAC can be extremely reduced at the cost of some error that might be introduced by RDAC.

In Fig. 2. VT and VB are top and bottom reference voltages which are correspondent to REFT5P0V and REFB of the top block in Fig. 1. VCM is almost half of the supply voltage which does not need to be exact value according to [4], in the switching scheme that we have applied. To reduce power consumption, the RDAC can be disabled for the period that signal is sampled or MSBs are decided.

III. Experimental Results

This 12-bits ADC is designed and simulated in a 90 nm complementary metal-oxide semiconductor process using spice models. The clock frequency is 120 MHz, and the conversion rate is 6 MS/s. The decision of the LSBs in RDAC are done in 2 clock cycles to reduce the settling errors. The supply voltage for this design varies from 2.7 V up to 5.5 V. Fig. 3, presents the layout of this ADC which shows the area occupation is as low as 240 µm × 240 µm.

Fig. 4a, shows the Fast Fourier Transform (FFT) spectrum with 4096 samples for 660 kHz input frequency and 5 V supply voltage. The effective number of bits (ENOB), signal to noise and distortion ratio (SNDR), and spurious free dynamic range (SFDR) for this simulation are 11.8 bits, 72.8 dB, and 90 dB, respectively. Fig. 4b, shows the FFT spectrum with 4096 samples with 92 kHz input frequency and 2.7 V supply voltage.

The ENOB, SNDR, and SFDR for this simulation are 11.2 bits, 69.2 dB, and 86 dB, respectively. This ADC consumes 980 µA at 660 kHz input frequency from a 5 V supply voltage (1.2 V for digital). Therefore, the Figure of Merit (FOM) for this ADC at the frequency of interest is 229 fJ/Conv.step according to the equation presented in [4].

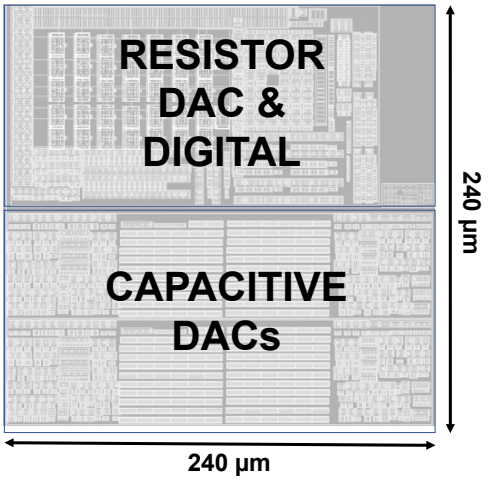
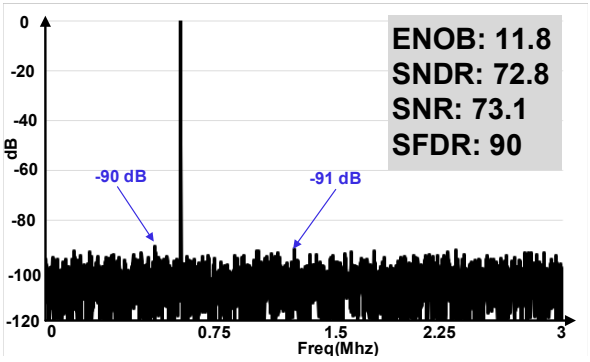
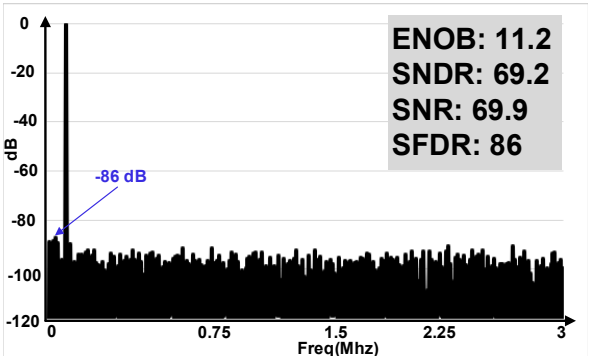


Fig. 3. Layout of the designed ADC



(a)



(b)

Fig. 4. FFT with 4096 number of samples a) 5 V supply voltage, 660 kHz input frequency, b) 2.7 V supply voltage, 92 kHz input frequency

IV. Conclusion

This paper presented a 12-bit SAR ADC designed for BLE applications. The contribution of this work was to reduce the number of capacitors in the CDAC. To achieve this, a hybrid type DAC has been applied where 8 MSBs were decided through CDAC and 4 LSBs were decided in a resistor DAC. The conversion speed for this design reached up to 6 MS/s. The prototype ADC was designed in a 90 nm CMOS process. The analog and digital supply voltage ranges for this design were 2.7–5.5 V and 1.1–1.3V respectively. For 6 MS/s conversion rate, this ADC achieved up to 11.8 and 11.2 ENOB, for the maximum and minimum supply voltages respectively. The current consumption from 5V supply voltage is 980 µA. The FOM for this design at the frequency of interest was calculated to be 229 fJ/Conv.step.

Acknowledgment

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