A Design of 20MS/s 12-bit Charge Sharing SAR ADC for Ultrasound Diagnostic Medical Devices

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***Abstract*— This paper presents the design and implementation of a 12-bit charge sharing analog-to-digital converter(ADC) composed of an integrated RF transceiver based on low noise, low area, and low power for ultrasound diagnostic medical devices. The proposed charge sharing DAC architecture consists of unit capacitor array and switches with low threshold voltage devices to minimize the size of the ADC. Thus, the proposed ADC had the size of 1600um x 505um with 130nm CMOS process. For the input frequency of 5MHz, the designed ADC had ENOB of 10.64-bit and SNDR of 65.82dB with the current consumption of 8.172mA for 8-channel.**

***Keywords*— charge sharing; SAR ADC; multiple channels; small area; low power consumption**

I. INTRODUCTION

With the advent of biomedical technology along with the aging society in the global medical market, the development of medical devices has been required increasingly. Medical devices, especially ultrasound diagnostic imaging medical devices, are constantly generating high demand and are growing into future-oriented industry. Ultrasound technology is expected to expand not only the general diagnosis area, but also the entire area of medical services such as prevention, treatment, and management. Also, it will be expanded to related industries and application technologies by developing the improved performance of the ultrasound imaging technologies.

However, the commercial medical portable ultrasound devices are limited in area due to ambient noise and their size, and power consumption are large since a lot of channels increase. Therefore, domestic portable ultrasound medical devices have difficulty in supporting high resolution and measuring a part of the measurable body. Through compact ultrasound diagnostic devices which improve the performance of the area and power consumption for the number of channels, the portability could be improved.

This work purposes an optimal ADC for an integrated ultrasound RF transceiver based on low noise, small area, and low power. Thus, the proposed charge sharing Successive Approximation Register(SAR) ADC for 8-channel has high resolution of 12-bit and high speed of 20MS/s to process the received signals from RF beamforming transceiver.

II. GENERAL STRUCTURE

A. Overview

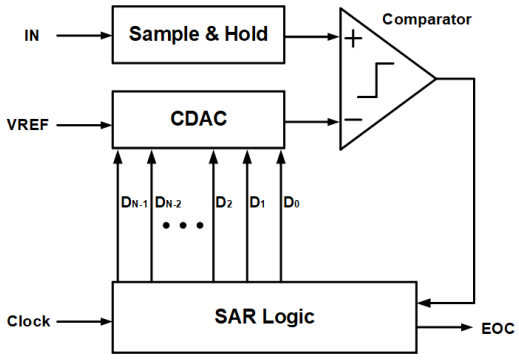

Fig. 1. A General Structure of SAR ADCs

A general SAR ADC is operated with binary search methods to use quantized conversion. SAR ADC consists of sample and hold circuit, capacitive DAC, a comparator, and SAR logic shown as Figure 1. It decides the allocated digital values through the sequential comparison from the most significant bit(MSB) to the least significant bit(LSB). The general SAR ADCs have conversion speed under a hundred of MHz and resolution under 14-bit, which has low power consumption with a small area.

B. Drawbacks

A conventional 20MS/s 12-bit SAR ADC needs a large number of capacitors in the capacitive DAC(CDAC), even though split-capacitor technology. It brings about difficulties to design ADCs with low power and high speed due to the large capacitors. The more capacitors are used, the more power consumption and the settling time increase. Thus, the operation of ADC, which determines bit values for each clock, has a difficulty to be quick. This work proposes a charge sharing SAR ADC structure which has so much less capacitors than conventional one. So it could have fast settling time for the low capacitance with a small area.

III. Proposed Structure

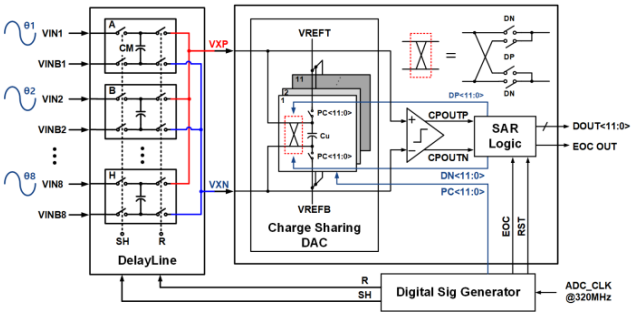

Fig. 2. The Proposed ADC Block Diagram

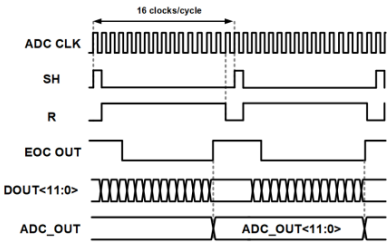

Fig. 3. The Proposed ADC Timing Diagram

Figure 2 shows the proposed charge sharing 12-bit SAR ADC, which consists of delay line circuits, a charge sharing DAC, a comparator, an SAR logic, and a digital signal generator. Delay line circuits are used for processing the input signals from the 8-channel at the same time. The ADC operates with the reference clock of 320MHz, and the digital logic generates SH and R signals with the period of 20MHz by using the reference clock shown as Figure 3. As SH and R signals are changed, the input signals are sampled and hold by delay line circuit. When R signal is high, the ADC converts the sampled signals to the allocated digital signals. After all conversion, End of Conversion(EOC) signal gets high to inform about the completion of the conversion. Through the EOC signal, the output data of ADC is sent to external modulator and demodulator.

A. Delay Line Circuits

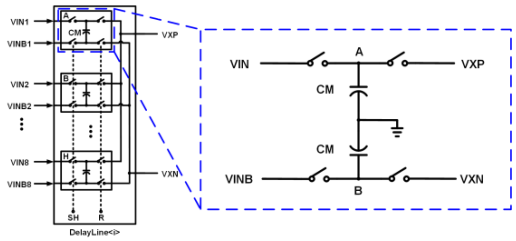

Fig. 4. 8-channel Delay Line Block Diagram

Delay line circuits receive 8-channel differential inputs. When the SH signal is high and the R signal is low, the input signal is stored at the capacitor of a unit memory cell(CM) in the delay line. When the SH signal is low and the R signal is high, it starts 12 times of conversion.

B. Charge Sharing DAC

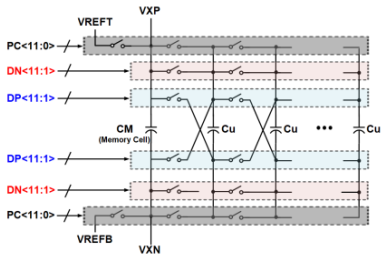

Fig. 5. Charge Sharing DAC Block Diagram

The charge sharing DAC is pre-charged by the two reference voltages of VREFT, VREFB on the MSB capacitor, and the rest of the capacitors is pre-charged by sharing their charge. The pre-charged capacitors share their charge to the CM, where the input signals are sampled. When the polarity of the comparator output is positive, the DP switch of the first bit turns on. When the polarity is negative, the DN switch of the first bit turns on. As the switches turn on, the output voltage of the DAC gets changed, and the outputs (VXP, VXN) are compared by the following comparator. It sequentially operates making a decision of the next bit until the last bit.

C. Comparator

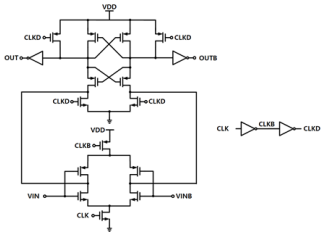

Fig. 6. The Schematic of the Dynamic Latech Comparator

The comparator makes a decision of the polarity, comparing the differential outputs of the DAC. And it sends the results to the SAR logic. Since the DAC outputs are also formed over a wide range of voltages, the performance of the comparator is required to deal with a wide range of input voltages. Thus, it is designed with NMOS and PMOS to operate on Rail-to-Rail. Using an inaccurate comparator in ADCs, missing code could be occurred by the higher offset of the comparator than 1 LSB. In this work, the comparator has a lower offset than 0.5 LSB. Figure 6 shows the schematic of the designed dynamic latch comparator.

D. SAR Logic

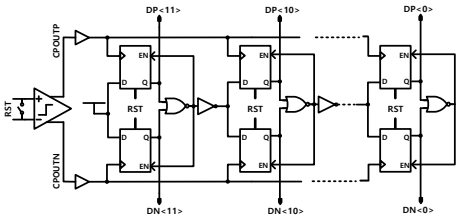

Fig. 7. SAR Logic Block Diagram

The proposed SAR logic adopts a synchronous structure to get high resolution ADC with the reference clock of 320MHz. A general high speed SAR logic has a large percent of high power consumption of SAR ADCs. To decrease the power consumption, it requires to be minimized. Figure 7 shows the block diagram of the SAR logic with a 12-stage differential shift register, which consists of a pair of D flip-flops with an enable input. It comes to the simplification of the design.

E. Digital Singal Generator

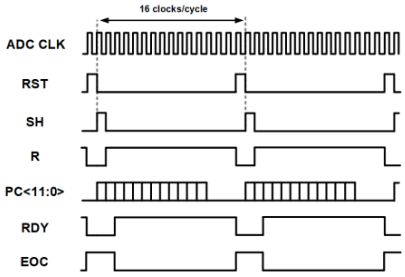

Fig. 8. The Proposed ADC Timing Diagram

The designed digital signal generator is operated with an external clock of 320MHz. It generates SH and R signal for the sampling, PC<11:0> for the pre-charge, RST for the reset, and EOC for the end of conversion. There are three reasons for generating digital signals independently. Since the input signals are sampled by the delay line circuits at the RF beamforming, SH and R signals requires to be independent from SAR logic. RST signal gets high before sampling to reset the capacitors and the digital values. PC<11:0> signals should be constant because different pre-charge signal lengths cause to fail the charge sharing. Therefore, these signals could be independently generated to operate accurately. Figure 8 shows the timing diagram of the digital signal generator.

IV. Simualtion Resuits

Figure 9 shows the FFT simulation results of the proposed charge sharing SAR ADC at the input frequency of 5MHz. It has ENOB of 10.64-bit, SNR of 70.06dB, and SNDR of 65.82dB with the current consumption of 8.172mA for 8-channel.

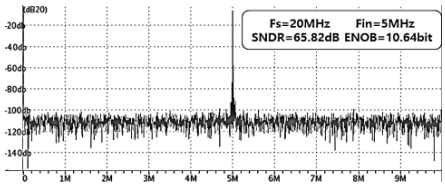

Fig. 9. The Simulation Results of the Designed SAR ADC

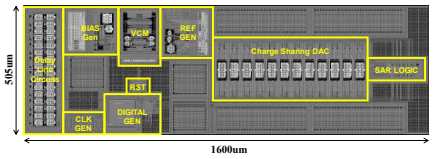

Fig. 10. The Layout of the Proposed SAR ADC

V. Conclusion

Table 1 shows the summary and comparison between the proposed ADC and the state-of-the-art SAR ADCs [3], [4] for ultrasound receivers. The proposed structure has high SNR and small area per channel while having the same sampling rates and resolution. For DAC, which has a high proportion of the size in ADC, the charge sharing structure significantly reduces the size by using a unit capacitor array. The proposed ADC has no small power consumption, but it has a high SNR for accuracy and a small area for portability. Thus, the proposed ADC is suitable for ultrasound imaging diagnostic medical devices.

TABLE I. Comparison of the State-of-the-Art ADCs

Parameters	[3]'18	[4]'19	This work
CMOS	65nm	180nm	130nm
Architecture	SAR	SAR	SAR
Resolution (bit)	12	12	12
Number of channels	24	8	8
Sampling rate (MS/s)	160	20	20
Peak SNR (dB)	47.8	60.1	70.06
Power/channel (mW)	1.1	2.6	1.5
FoM (fJ/step)	1.679	31.74	18.70
Area/channel (mm2)	N/A	0.284	0.101

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