High Efficiency & Low Area DC-DC Buck Converter with the Digital Feedback Loop for the Wireless Applications

Hyunjin Jeong
Department of Electrical and Computer Engineering
Sungkyunkwan University
Suwon, South Korea
jine1550@skku.edu

Kang-Yoon Lee
Department of Electrical and Computer Engineering
Sungkyunkwan University
Suwon, South Korea
klee@skku.edu

***Abstract*— In this Paper, a high efficiency and low area dc-dc buck converter with the digital feedback loop is proposed for wireless device. The digital feedback loop is consisted of two-step digital pulse width modulation (DPWM) and low power self-tracking zero current detector (ST-ZCD). To implement a high-efficiency dc-dc converter, a hybrid DPWM core is proposed with high linearity and low power consumption. To reduce the output voltage ripple within 20mV, an adaptive window analog-to-digital converter is proposed. To minimize the reverse current, a dead time generator is implemented with the proposed ST-ZCD. The circuit is designed with a Samsung 28nm CMOS process that produces an output voltage of 1.8V using a standard supply voltage of 3.3V.**

***Keywords*—Adaptive window ADC, Buck converter, DPWM, ST-ZCD.**

I. INTRODUCTION

Recently, as the wireless application has been actively developed, it is necessary to develop low-power and low-area circuits. However, battery life and charging technologies have not been developed enough to be suitable for wireless applications, and there is a growing interest in developing low-power power management technologies. When using a digital feedback loop, it has superior performance in a low-power DC-DC buck converter compared to using an analog feedback loop, and it is easy to obtain adequate transient performance. In the case of a conventional DC-DC converter, zero-current is detected through the internal switching node (V_X). At this time, a voltage drop occurs due to the MOSFET, and since the existing ZCD uses a high-performance comparator, the power consumption is significant. Therefore, in this paper, we use Adaptive Window Analog-to-Digital Converter (ADC) and Self-Tracking ZCD (ST-ZCD) to compensate for this problem. The use of an adaptive window ADC reduces the output ripple voltage, and the use of ST-ZCD can significantly reduce power consumption.

II. STRUCTURE OF DPWM DC-DC CONVERTER

Fig. 1 is the conventional block diagram of the DPWM dc-dc buck converter.

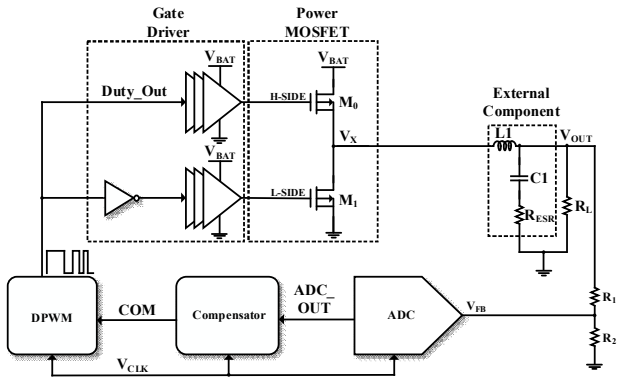

Fig. 1. Block diagram of Conventioal DPWM dc-dc buck converter.

The DPWM generates digital pulses that control the ON/OFF time of the power MOSFET switch during the switching period. In this way, the output voltage (V_{OUT}) is adapted to the proper value [1]-[2]. Fig. 2 (a) and (b) are respectively the block diagram of prevalent DPWM consisting of the counter-based method and the delay line based method for duty control of power MOSFET gate signals. Among them, the counter-based method can achieve high resolution and excellent linearity. On the other hand, since the clock frequency increases in proportion to the number of bits, the current consumption increases [5]. With the delay line-based method, it has a disadvantage about the linearity with PVT variations. Also, in a delay line based DPWM, if the delay has to be increased, the area needs to be increased as well. In General, the counter-based method demands high linearity, so high frequency is required. For this reason, it consumes an enormous volume of current.

Typically, the compensator for the dc-dc buck converter is implemented by external devices [6]. Thus, the compensator of the conventional structure has several problems about a large area and current consumption. Therefore, the conventional DPWM dc-dc buck converter is less efficient due to the high power dissipation, large area, and low switching frequency of each block [3].

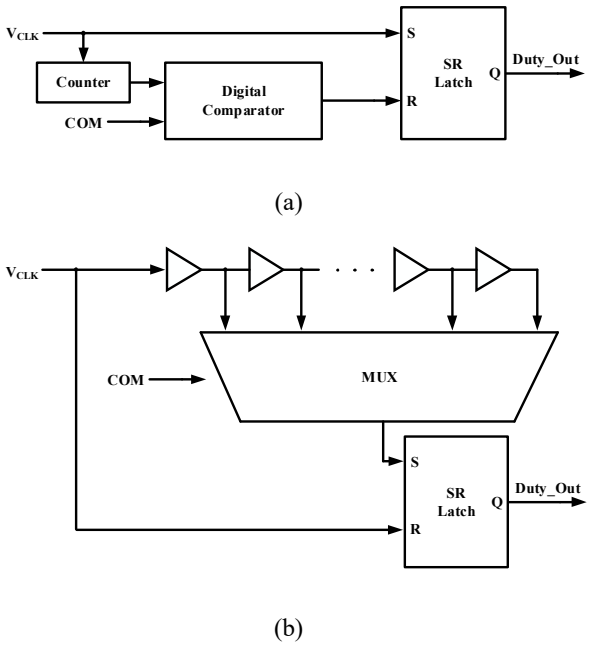

Fig. 2. Block diagram of the prevalent DPWM with counter (a) and delay line based (b) method.

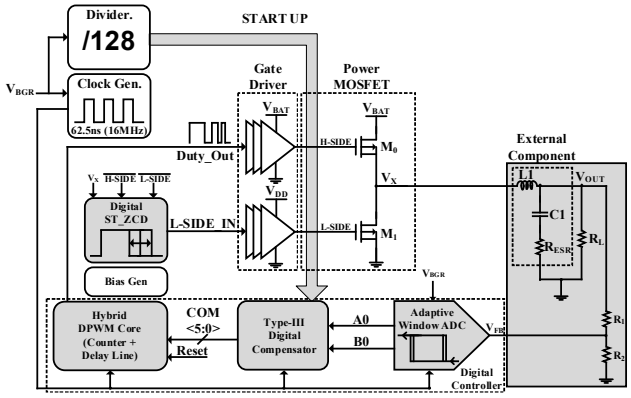

Fig. 3. Block diagram of the DPWM dc-dc buck converter.

Fig. 3 is a top block diagram of the dc-dc converter with the digital feedback loop that proposed in this paper. It receives the feedback voltage from adaptive window ADC and processes the data with the digital compensator to make 6-bit data (COM<5:0>) that determines the duty of the pulse. It makes gate control signal using the hybrid DPWM and prevents reverse current using the ST-ZCD.

III. Designed Blocks

A. Hybrid DPWM Core

Fig. 4 is a block diagram of the hybrid DPWM core. The hybrid core receives 6 bits of duty information from a type-III digital compensator. With this information, a signal that controls the gate is created.

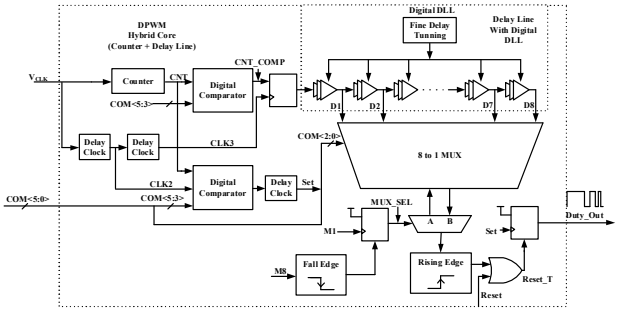

Fig. 4. Block diagram of the hybrid DPWM.

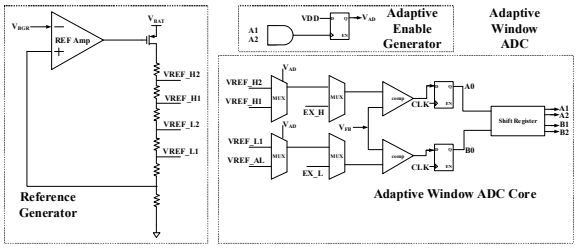

Fig. 5. Block diagram of adaptive window ADC.

MSB 3 bits are used to count 16MHz clock and LSB 3 bits are used for delay signal selection generated through delay cell. The DPWM dc-dc converter switching frequency is set to 2 MHz, and the clock frequency (f_{CLK}) is set to 16MHz for clock counting with MSB 3 bits. Each delay cell is set to 7.8ns (≈500ns/64) to control the duty using a delay cell with LSB 3 bits.

B. Adaptive Window ADC

Fig. 5 is a block diagram of the adaptive window ADC. In order to achieve high efficiency with low resolution, the Adaptive Window ADC is designed to operate only near the ideal feedback voltage, and the feedback voltage is interpreted in the time axis. The Adaptive Window ADC compares the reference voltage and the feedback voltage through a comparator. After a certain period of time, when the ripple voltage is stabilized by the adaptive window ADC, the width of the window is reduced using the AD signal to decrease the output ripple voltage to inside about 20mV.

C. Digital Self-Tracking Zero Current Detector (ST-ZCD)

Fig. 6 is a block diagram of the digital ST-ZCD. The ST-ZCD detects zero current by receiving voltage from V_X node. When the V_X voltage goes down to negative voltage, reverse current flows, so turn off the low side NMOS switch to prevent reverse current from flowing [4]. It generates UP, DOWN, and STAY signals based on the information from the V_X node, and determines the duty of the low side NMOS based on these signals. Similar to the hybrid core, a delay cell is selected to determine the duty of the low side. To make a more accurate pulse, the delay cell has a resolution of 6ns.

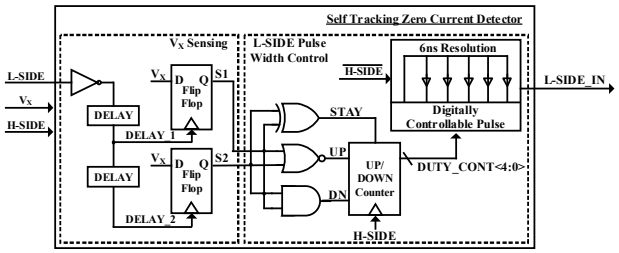

Fig. 6. Block diagram of the digital ST-ZCD.

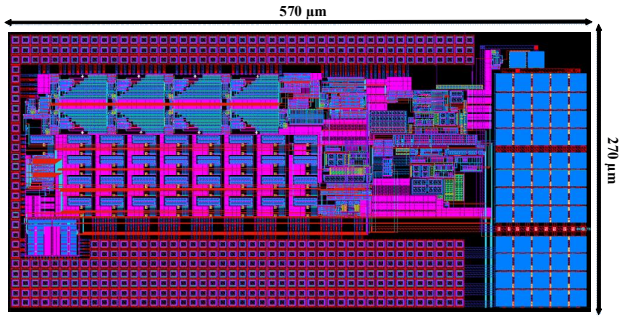

Fig. 7. Top layout of the DPWM dc-dc buck converter.

IV. Experimental Results

Fig. 7 shows the top layout of the dc-dc buck converter with the digital feedback loop. The top layout is designed in the Samsung 28nm CMOS process. The area of the dc-dc buck converter with the digital feedback loop is 570µm × 270µm.

Fig. 8 shows the simulation results of the proposed dc-dc buck converter with the digital feedback loop. The output ripple voltage is broadly 20mV. The switching frequency of the dc-dc buck converter with the digital feedback loop is 2MHz.

V. Conclusion

Through this design, it is possible to design the dc-dc converter with the digital feedback loop that has high power efficiency and good regulation performance. As the importance of the efficiency required for power management IC's is increasing, power is decreasing. In this situation, the above study is expected to be useful in situations where high value and especially low-area, low-power is required, such as wireless applications. Through the subsequent research process, inrush current improvement and appropriate ADC resolution will be obtained.

The proposed dc-dc buck converter with the digital feedback loop is designed in the Samsung 28nm CMOS process and produces an output voltage of 1.8V using a standard supply voltage of 3.3V. The total top layout area is 570µm × 270µm. The efficiency of the dc-dc buck converter with the digital feedback loop is 92%.

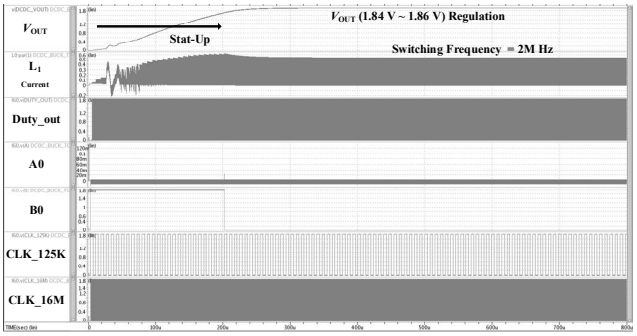

Fig. 8. Simulation results of the DPWM dc-dc buck converter.

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