Design of Frequency Multiplier with Delay Locked Loop that is insensitive to PVT Variation and prescreen Harmonic Lock

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***Abstract*— As the wireless network market has been grown, high-performance and efficient communication technology are demanded for devices. Specifically, reference clock signal forms an essential part of designing devices such as wearable one or the Internet of Things. The conventional structure of XOR is used to multiply the reference frequency. The structure of DLL illustrates that how frequency is extracted from application based on various values of desired supply voltage.**

Keywords—Frequency Multiplier, Delay Locked Loop

I. INTRODUCTION

These days, With the development of the wireless network market, the demand for devices such as high-performance microprocessors and more efficient communication methods has increased. In particular, when designing a wearable device or the Internet of Things(IoT), the reference clock signal is considered very important. The conventional structure most commonly used to multiply the reference frequency is designed using XOR. The structure shown below must operate at the desired supply voltage while providing the appropriate speed for the intended application

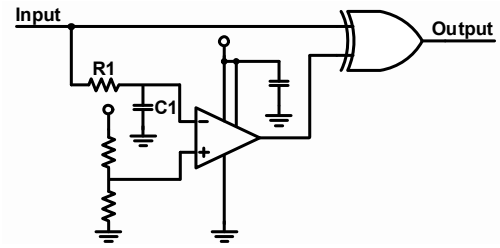


Figure 1. The conventional structure using XOR gate

R_1 and C_1 shown in the figure above are determined by the following equation.

$$R_1 \times C_1 = \frac{2}{3} \times \frac{1}{f_{DOUBLE}}$$

Where f_{DOUBLE} is the desired output frequency (twice). However, it reacts sensitively to PVT and it is difficult to operate normally as a multiplier depending on the temperature. To overcome this, a Delay Locked Loop (DLL) is formed using a Phase Frequency Detector (PFD), Charge Pump (CP), and Loop Filter (LF) based on the Voltage Controlled Delay Line (VCDL), and the First Phase Canceller (FPC) at the front end. It is designed to have good performance in the desired frequency band by preventing Harmonic Lock through.

II. MDLL ARCHITECTURE

A. Multiplying Delay Locked Loop Top Block Diagram

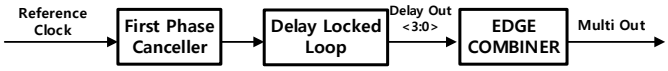


Figure 2. Top Block Diagram of MDLL

Figure 2 is the Top Block Diagram of MDLL. First, it prevents Harmonic Lock through FPC for two incoming signals, sends a signal, detects the difference between phase and frequency in an analog type PFD, and transmits UP / DOWN signals to CP. Then, The CP is passed to the VCDL through the LF and provides feedback. Delayed signals excluding the feedback signal in VCDL are transmitted to the Edge Combiner, and the frequency is doubled through the internal MUX and D-Flip Flop.

B. Voltage Controlled Delay Lines

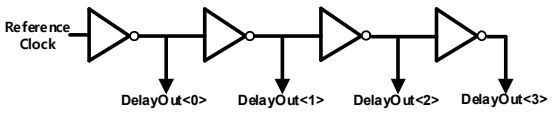


Figure 3. Schematic of VCDL

Figure 3 is the schematic of VCDL. Delay of signal is created by using current-starved inverter and shunt-capacitor and provided to DLL initial signal and Edge Combiner through alignment of first signal (Reference Clock) and last signal (DelayOut<3>) among them.

C. First Phase Canceller

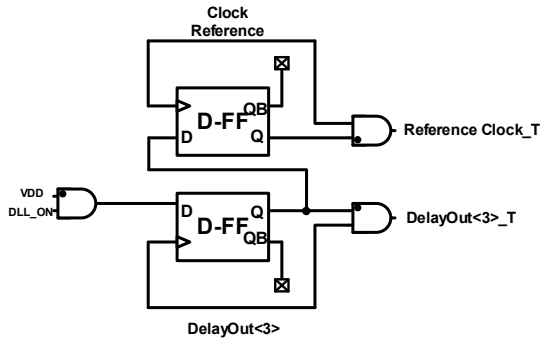
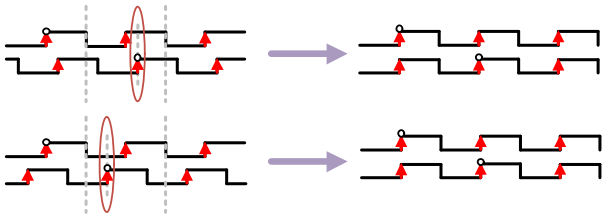


Figure 4. Schematic of First Phase Canceller

Figure 4 above is the schematic of the First Phase Canceller. To prevent Harmonic Lock, the figure must be satisfied with the following equation.

$$T_{CLK} < T_{VCDL\_MAX} < T_{CLK} \times 1.5$$

$$T_{CLK} \times 0.5 < T_{VCDL\_min} < T_{CLK}$$



In order to align the two signals, if they are not within the range, they are aligned with the wrong signal, causing Harmonic Lock. Therefore, by removing the initial phase of one of the two signals being compared, it is possible to help align the two signals to prevent harmonic lock.

D. Phase Frequency Detector, Charge Pump, Loop Filter

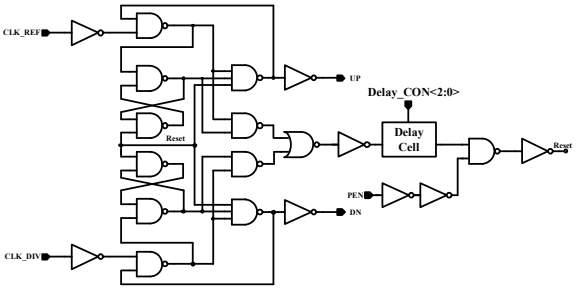


Figure 5. Schematic of PFD

Figure 5 above is the schematic of the PFD. In the above PFD, a structure in which Reset Delay Cell is added to prevent CP Dead Zone is used.

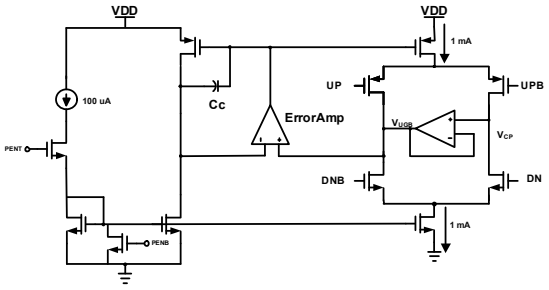


Figure 6. Schematic of CP

Figure 6 above is the schematic of the CP. CP can design the mismatch between UP and Down Current to less than 1%, and the signal transmitted through CP is transmitted to VCDL through LF.

E. Edge Combiner

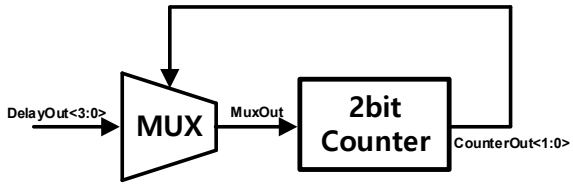
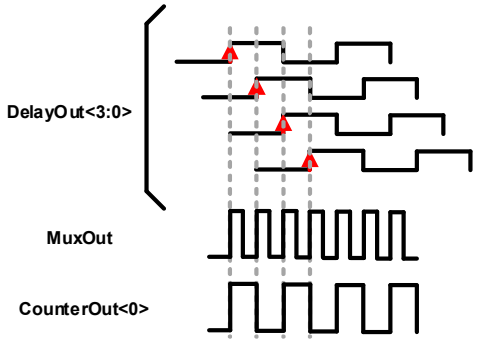


Figure 7. Block Diagram of Edge Combiner

Figure 7 above is the Block Diagram of Edge Combiner. It generates a signal that doubles the input frequency by using a 4x1 MUX and a 2bit counter.



The above operation recognizes the rising edge of all signals using 4×1 MUX for 4 signals transmitted from VCDL, and finally detects a signal with a frequency of 4 times made into one signal (MuxOut). After that, a feedback signal used for MUX, including a signal doubled to the input signal, is obtained from the 2bit Counter

III. SIMULATION RESULT

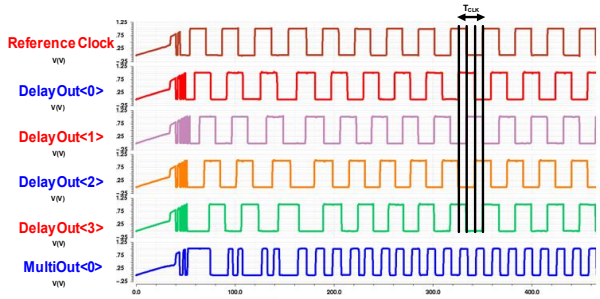
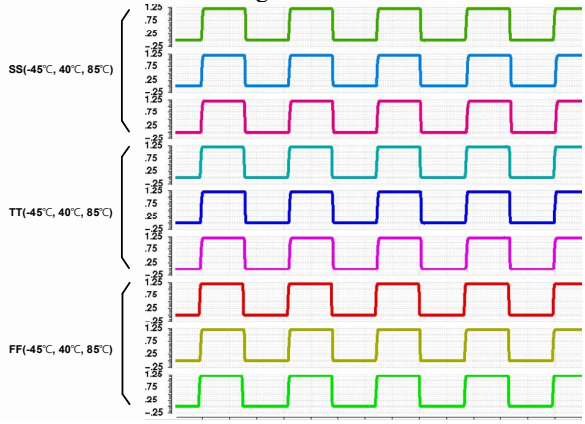


Figure 8. Simulation Result of MDLL

Figure 8 above is based on a supply voltage of 1.2V, and the input clock frequency is implemented at 30.72MHz. Through the FPC located at the front of this structure, the signal entering the Edge Combiner was confirmed by preventing the Harmonic Lock. As a result, it was confirmed that the frequency was doubled to 61.44MHz through the Mux and Counter.



Corner Simulation	Temperature (℃)		
	−85	40	−45
FF	ALL Pass		
TT			
SS			

As mentioned in the introduction, for PVT Variation, which was pointed out as a disadvantage in the conventional structure, this structure can check normal operation from -45℃ to 85℃ in FF/TT/SS.

IV. CONCLUSION

In this paper, we propose an MDLL structure that is insensitive to PVT Variation and generates a signal that is twice the reference frequency through comparison of two input signals. It was shown that the output frequency became 61.44MHz through the 1.2V supply power and the input frequency of 30.72MHz used in the simulation result, and it operates normally. In addition to these results, it is possible to create a frequency that is multiplied higher than 2 times or 4 times by adding cells inside the VCDL, and the output frequency can be multiplied for the input frequency in a wider band through the change of the shunt capacitor. Compared to the conventional structure using the XOR gate, since many devices and blocks are used and the size is increased, there is a need for a method that can be more effectively applied to an integrated circuit in the future. This process used an RF CMOS 55nm process.

ACKNOWLEDGMENT

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