A High Power High Efficient 5.8 GHz CMOS Class-A Power Amplifier for a WPT Application

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Abstract— This paper presents a high power and highly efficient 5.8 GHz differential two-stage cascode Class-A Power Amplifier (PA) for a Wireless Power Transfer (WPT) system. The PA is designed in a standard General Purpose (GP) 180 nm CMOS technology. The process does not apply any Radio Frequency (RF) devices such as inductor nor transformer which are essential for an RF design. A full custom-made transformer is proposed and optimized at 5.8 GHz which is modeled using EMX analysis. The proposed transformer shows 1.5 nH and 1.28 nH inductance at the primary and secondary sides of the transformer while their quality factor reaches up to 11.4 and 11 at 5.8 GHz, respectively. Even though reaching higher efficiencies in CMOS processes is more challenging than the GaN processes, the proposed PA has a relatively high Power Added Efficiency (PAE) of 33%. The power gain of the PA is 19.47 dB at 5.8 GHz. The average current consumption of the PA is 144 mA while the power supply is 1.8V.

Keywords—PA, 5.8 GHz, High-Power, WPT

I. Introduction

Recently, Internet of Things (IoT) applications, wearable devices such as smartwatches, and a wide variety of mobile applications like smartphones and ultra-books are used, drastically. Therefore, a wide field of research is provided for the researchers to enhance various technologies to recharge the devices. Technologies such as Quick Charge (QC) and Wireless Power Transfer (WPT) are the most applicable enhances in recent years [1].

The pace of the energy-efficient circuit design has been much more than the improvement in battery design technology for mobile devices in recent years. Therefore, this gap must be filled by enhancing newer technologies to recharge the slow batteries with a higher speed and ease of access. To meet fast charging with a high accessibility a wireless charger based on the WPT technology with a high output power is interesting [2]. To enhance wireless charging technology, two methods are suggested. Wireless charger using a magnetic coil and using a single-ended antenna. The magnetic coil wireless chargers are used when the charge receiver device is in touch with the charger. A wireless charger with a single-ended antenna is used to charge the receivers which are far from the charging source.

In this paper, a Power Amplifier (PA) is proposed for a WPT application. The proposed PA is implemented with a differential input and a single output that is connected to the antenna. The operating frequency of the PA is at 5.8 GHz which is the frequency of the Phase Locked Loop (PLL). The proposed PA must perform an efficient operation with a limited amount of current consumption. The target of the design is to reach more than 19 dBm when the minimum input power of the PA is 0 dBm. A Power Added Efficiency (PAE) of more than 30% is also required for the PA.

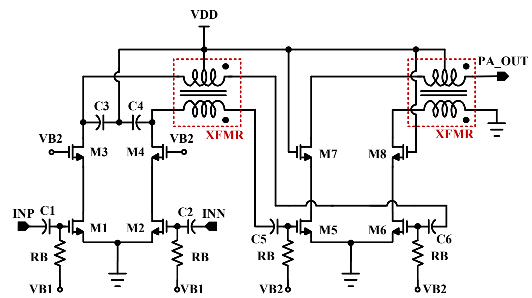

Fig. 1. The proposed differential two-stage cascode Class-A Power Amplifier (PA)

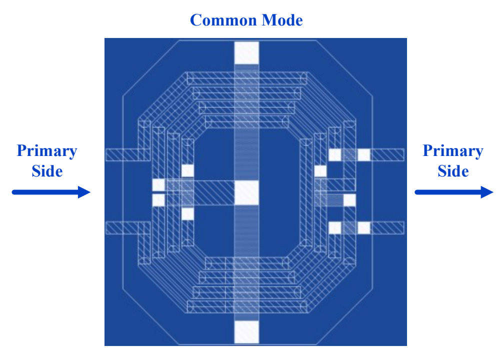

Fig. 2. The fully custom-made transformer.

II. Structure

A. Circuit Implementation

The proposed PA is a differential two-stage cascode Class-A type, where the first stage (the driver) is fully differential, and the second stage is single-ended (Fig. 1). The first stage has a lower power gain compared with the second one. This stage is called the driver stage where the input transistors are much smaller than the second stage. This causes a less loading effect on the previous block (PLL). The second stage is formed of much larger transistors and higher power gain capability. The cascade bias of the second stage is directly connected to the VDD but for the driver stage the cascade bias is lower than VDD to keep the power gain of the first stage limited.

The transformers (XFMR) are fully custom made and their model is extracted by the EMX analysis. Fig. 2, shows the drawn custom XFMRs. Fig. 3 and Fig.4, show the simulation of the inductance (L) and quality factor (Q) of the primary and secondary sides of the XFMRs at 5.8 GHz, respectively. The obtained Q and L for the primary and the secondary sides of the XFMR are satisfying to provide the required specs.

III. Experimental Results

The proposed PA is designed in a standard General Purpose (GP) 180 nm CMOS technology. Fig. 5, shows the top layout of the PA including the input/output (I/O) pads. The core of the PA occupies 400µm×1100µm. Fig. 6, shows the load-pull simulation which is for output maximum power matching. To enhance the output matching a T-matching network is designed based on the load-pull simulation.

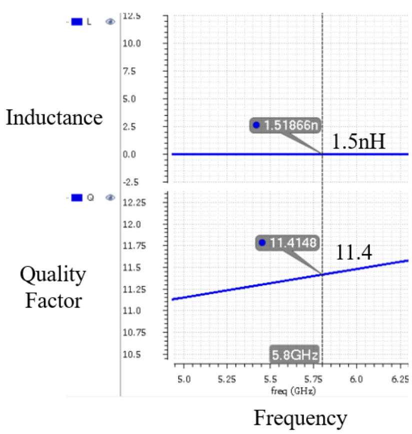

Fig. 3. The inductance and the quality factor of the primary side of the XFMR.

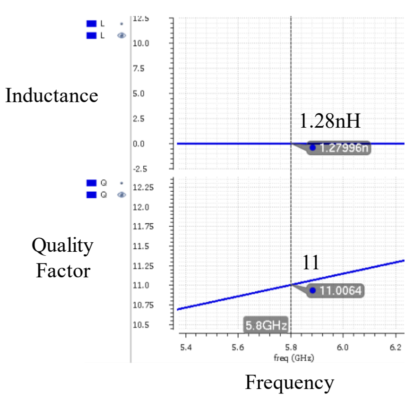

Fig. 4. The inductance and the quality factor of the secondary side of the XFMR.

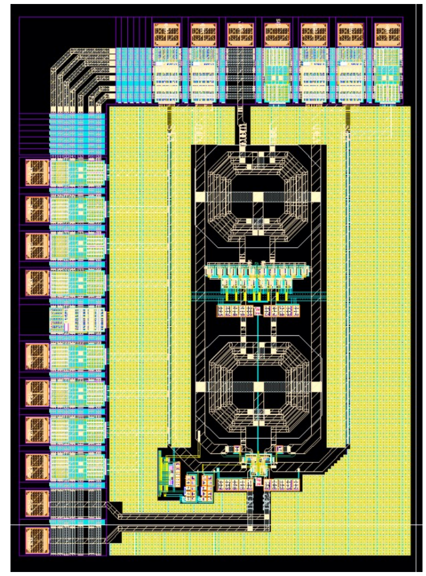

Fig. 5. Top layout of the proposed PA.

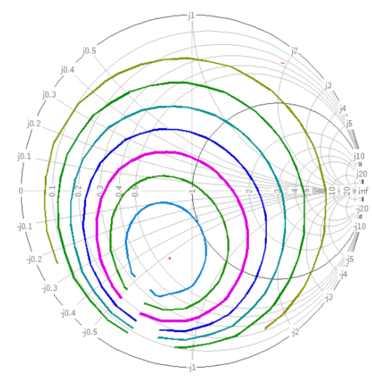

Fig. 6. The load-pull simulation of the PA.

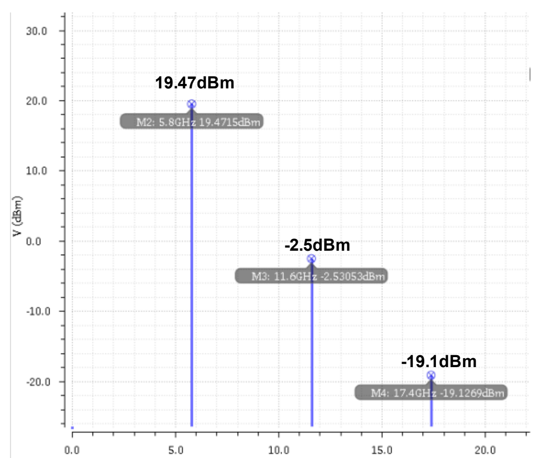

Fig. 7. Output harmonics of the PA.

Fig. 7, shows the PSS simulation results of the PA which is reflecting the output harmonics of the PA when the input power is 0 dBm. Mainly, a maximum power gain and a high PAE dictate the spec of the PA for a WPT application. Fig. 8, shows the transient results of the output voltage at the antenna (ANT) and the current consumption of the PA which is 144 mA on average. Fig. 9, shows the PAE of the PA versus the input power levels which reflects a high PAE around 33% at 5.8 GHz. Fig. 10, shows the Output 1-dB Comparison Point (OP1dB) which results in a 16.7 dBm. Fig. 11 and Fig. 12, shows the OIP2 and OIP3 of the PA, respectively and Table I, presents a performance comparison for this work and recent papers.

IV. Conclusion

A 5.8 GHz differential two-stage cascode Class-A PA is designed in a standard 180 nm GP CMOS technology. The power gain of the PA reaches up to 19.4 dB with a 33% PAE while 144 mA is the current consumption from a 1.8 V power supply.

Acknowledgment

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TABLE I. Comparision Table

	Frequency	Pout	PAE	Process
[4]	5.8GHz	41.2dBm	68.7%	$GaN\ HEMT$
[5]	4.8GHz	343W	53%	GaN
[6]	5GHz	100W	31%	$GaN\ FET$
This Work	5.8GHz	19.47dBm	33%	$CMOS$

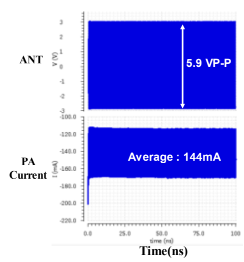

Fig. 8. Transient analysis of the current consumption and the output signal at ANT of the PA.

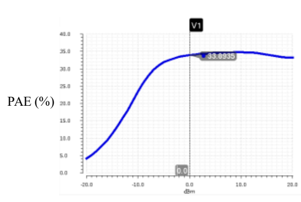

Fig. 9. The PAE of the PA versus the input power.

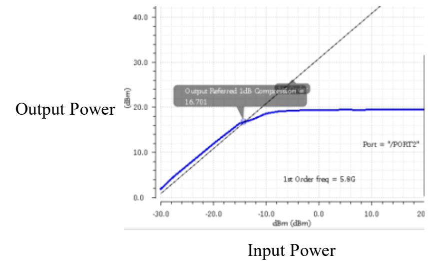

Fig. 10. The OP1dB of the PA.

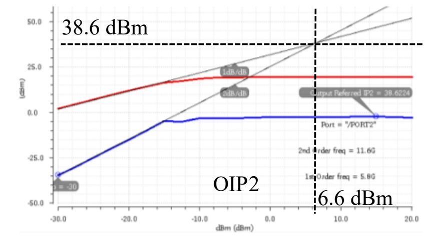

Fig. 11. OIP2 of the PA

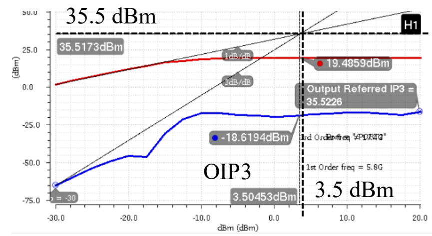

Fig. 12. OIP3 of the PA

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