Design of Baseband Analog with Filter Tuning for 5.8GHz DSRC Transceiver in ETCS

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***Abstract*—** This paper introduces a design of baseband analog with high performance IRR (Image Rejection Ratio) to using wide-bandwidth for DSRC (Dedicated Short Range Communication) transceiver. In addition, an automatic filter tuning system has applied to in this circuit for higher PVT tolerance and accuracy of bandwidth. To reduce adjacent interferers and image signal in baseband circuit, Complex Band Pass Filter (BPF) is used in this system. Baseband analog has high performance of IRR 66.5 dB at 3-dB bandwidth and the Intermediate Frequency (IF) are 10MHz. This circuit is designed in 130nm CMOS process. Power consumption is 7.46mW under 1.2V power supply.

Keywords— Wideband, DSRC(Dedicated Short Range Communication), Complex Band Pass Filter, Automatic Filter Tuning System

I. INTRODUCTION

Recently, the Electronic Toll Collection System (ETCS) is being implemented worldwide. DSRC is one of the methods for providing a system in a short-range wireless communi cation method for Intelligent Transport System (ITS). As wireless communication services and technologies for vehicles advance, DSRC systems require high-performance RF circuits for signal processing. In particular, video signals and adjacent interferers deteriorate the transceiver's performance, so filtering is required. Also, with low power, the circuit becomes more sensitive to PVT variation such as active capacitors. The filter tuning circuit control the capacitor in complex BPF by checking the charging time of capacitor. Then the capacitance becomes almost constant over the PVT variation. In this paper, we design a baseband analog with automatic filter tuning system for DSRC transceiver.

II. PROPOSED ARCHITECTURE

A. Top block Diagram

Fig. 1 shows the proposed baseband analog block diagram. It is constructed of three VGA (Variable Gain Amplifier), two 2nd order BPF, and two DCOC (DC Offset Canceller). The input signal of the baseband analog is output of RF front-end down-mixer. The complex BPF is good at reducing adjacent interferers and image signal for low IF receiver.

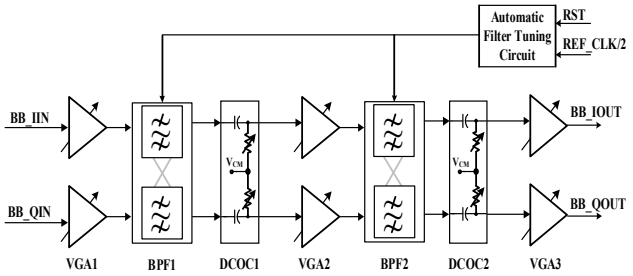

Fig. 1. Proposed baseband analog block diagram

The designed baseband analog amplifies and filters the Quadra ture signal. VGA and complex BPF receive I, Q, IB and QB as inputs and outputs by configuring fully differential type. The DCOC changes DC offset voltage of BPF output. It is consi sted of capacitors and resistors and forms high pass filter to coupling AC voltage.

B. Complex Band-pass Filter

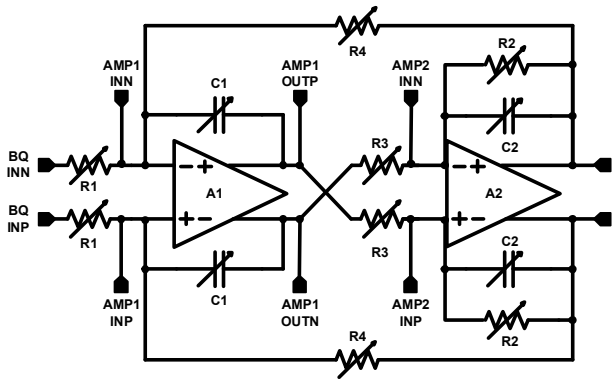

Fig. 2. The structure of 2nd order BQ filter

Fig 2 shows the design of BQ (bi-quads) filter. The filter is designed by using a reverted Thomas Tow filter. This structure can control gain and bandwidth of band-pass filter. The gain of BQ filter is calculated by the ratio of R1 to R4. The gain may be larger if smaller R1 resistance is connected.

$$A_V = \frac{R_4}{R_1} \tag{1}$$

Bandwidth of the filter is determined by capacitances of C1 and C2. As using smaller capacitances of C1 and C2, the bandwidth become wider. But wide bandwidth may cause voltage gain drop. In order to preserve constant gain, the bandwidth of VGA has to be wide. The ripple of bi-quad filter is obtained by resistance of R2. Fig. 3 shows the proposed complex BPF. This complex BPF attenuates the image tones of I / Q signal by cross-coupled resistors. The input of I and output of Q signals are connected to design feedback loop. Checking stability of this loop is important to prevent oscillation of BPF.

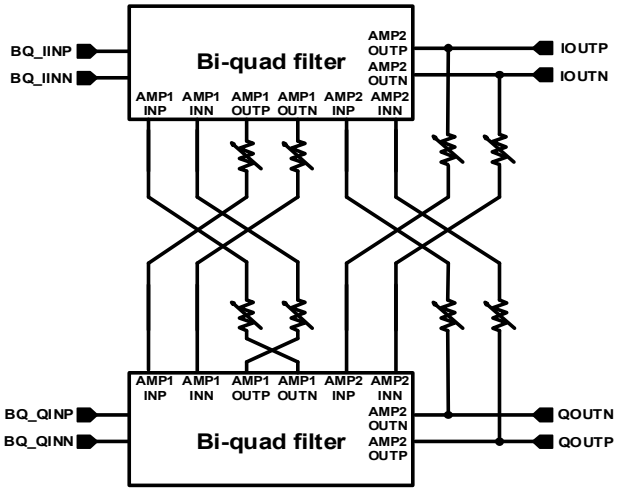

Fig. 3. Structure of complex Band Pass Filter

C. Automatic Filter Tuning Circuit

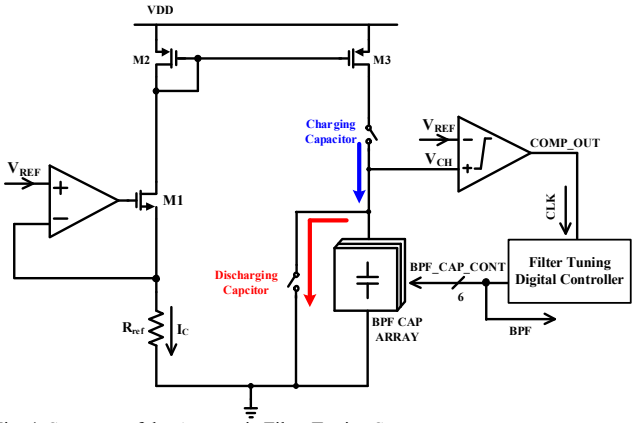

Fig. 4. Structure of the Automatic Filter Tuning System

Fig. 4 shows circuit of the automatic filter tuning system. It is constructed of capacitor array and current mirror part and filter tuning digital controller part. Capacitor array and current mirror part generate charging voltage. Digital controller check s output of the comparator and changes the capacitance. Capa citor array in filter tuning circuit is in the complex BPF.

I_C charges C_{ARRAY} and generate V_{CH} with time delay (t_d) simultaneously. Then, we gave to consider the equation below

$$Q = I_C \cdot t_d = C_{ARRAY} \cdot V_{REF}$$

If capacitance of C_{ARRAY} is changed by PVT variation, charging time of capacitor is changed by variation of capa citance. Then, digital controller senses the difference value between V_{CH} and V_{REF} and changes capacitance of C_{ARRAY} in complex BPF.

III. Experimental Result

A. Layout

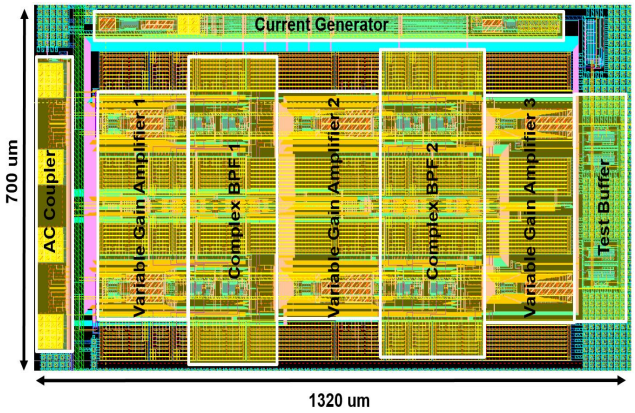

Fig. 5. Layout of Proposed Baseband Analog

Fig. 5 shows the layout of the proposed BBA with auto matic filter tuning system circuit. The total layout area including test buffer is 700um * 1320um. In this paper, 130 nm CMOS process is used. To avoid I / Q mismatch, layout was done as symmetric as possible.

B. Simulation Results

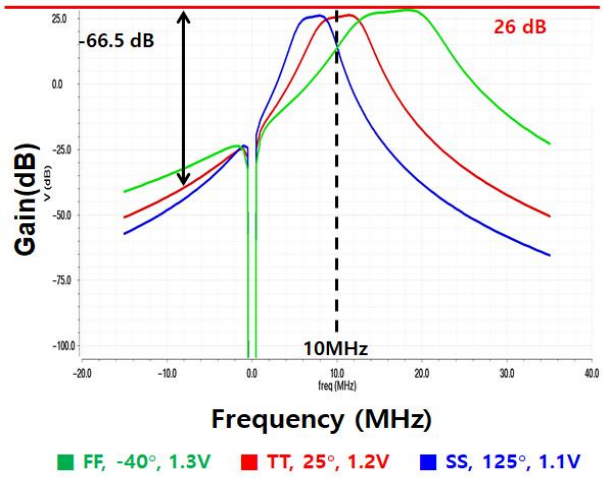

Fig. 6. AC simulation with filter tuning off of Proposed Baseband Analog

Fig. 6 and Fig. 7 show the ac response of proposed baseband analog ac simulation with Automatic Filter Tuning on and off. When filter tuning is turned off, center frequency and bandwidth changes under PVT variation. However, when filter tuning is turned on, stabilizes the filter shape and reduces the change.

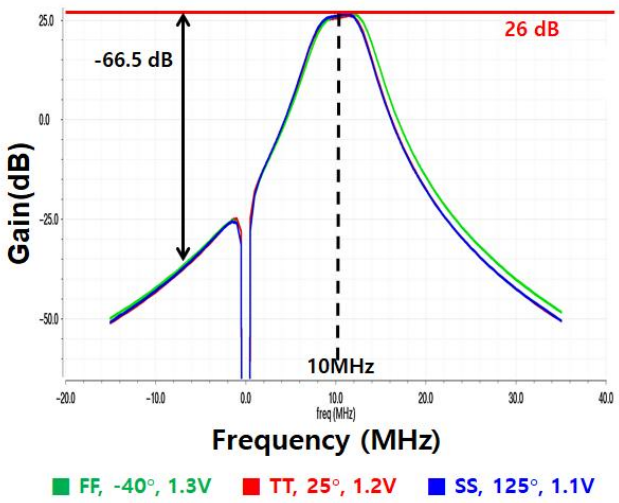

Fig. 7. AC simulation with filter tuning on of Proposed Baseband Analog

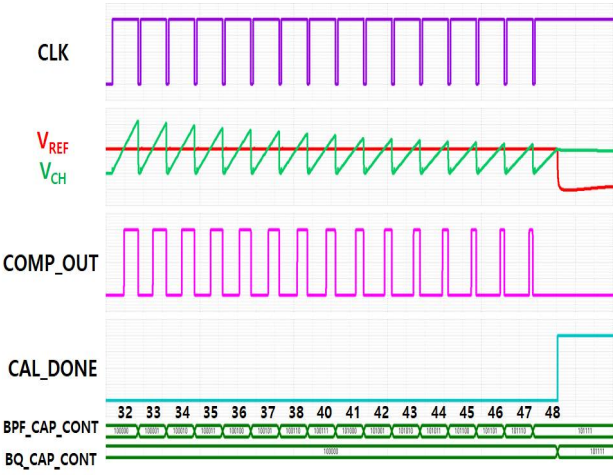

Fig. 8. Automatic Filter Tuning Circuit processing flow diagram

Fig. 8 illustrates the processing flow of automatic filter tuning circuit. CLK charges the C_{ARRAY} in rising edge and discharges the C_{ARRAY} in falling edge. Furthermore, value of capacitance is changed due to PVT variation, therefore, charging time also will be either short or long.

Only if V_{CH} is higher than V_{REF}, COMP_OUT is on. When the on-time of the COMP_OUT is shorter than initial delay, Calibration is over and CAL_DONE is on. Before CAL_DONE is turn on, BPF_CAP_CONT increases every single CLK. If CAL_DONE is on, digital controller changes control bit to BPF_CAP_CONT. With this progress, the capacitance in capacitor bank can be constant under the PVT variation. It makes the circuit get higher PVT tolerance.

IV. Conclusion

In this paper, we proposed baseband analog with automatic filter tuning system. The proposed baseband analog is consisted of three stages of VGA, two 2nd order BPF, and two DCOC. The IF is 10MHz and bandwidth is 4MHz. The max gain of baseband is 26dB and image rejection ratio is 66.5dB. To reducing power consumption, the input MOSFETs are operated in subthreshold region in VGA and complex BPF. 130 nm CMOS process is used and total power consumption is 7.46mW.

TABLE I. Perfomance summary of baseband analog

Parameter	Value
Process	130nm CMOS
Supply Voltage (v)	1.2
Max Gain (dB)	26
Bandwidth (MHz)	4
Image Rejection Ratio (dB)	66.5
Power Consumption (mW)	7.46
Area (mm^2)	0.924

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