High-efficiency, High-power Class-D Power Amplifier with 50W Output Using GaN Devices

Yeun Jeong Park
Department of Electrical and Computer Engineering,
Sungkyunkwan University
Suwon, Republic of Korea
duswjd6724@g.skku.edu

Kang-Yoon Lee
Department of Electrical and Computer Engineering,
Sungkyunkwan University
Suwon, Republic of Korea
klee@skku.edu

***Abstract*— GaN (Gallium nitride) semiconductors have more than 10 times the power density of Si-based Latterly Diffused Metal Oxide Semiconductor (LDMOS) transistors used in conventional Power Amplifiers, enabling more than 30% power savings and higher power density and efficiency. In this paper, we design a high-efficiency, high-power Class-D Power Amplifier with output higher than 40W by controlling the full-bridge structure composed of GaN elements using GaN drivers. The proposed Power Amplifier uses the Samsung 180nm process and designs 5 V as supply power.**

Keywords*— *Full-Brigde GaN core, High Efficiency, Class-D Power Amplifier, Dead-Time Geverator, Voltage Control Delay Loop(VCDL)

I. Introduction

Recently, next-generation communication systems such as WiMAX and LTE have transmitted from simple voice signals to complex signals for multimedia communication for video transmission and Internet access. The characteristic of these wireless communication system signals is that they have high peak-to-average power ratio (PAPR) as well as broadband characteristics.

Designed to transmit power from these features, Power Amplifier serves to amplify power at low power efficiency and send it to atmosphere. The low-efficiency characteristics of the Power Amplifier deepen the heat generation of the power amplifier itself, exacerbating the reliability and characteristics of the mobile communication system. To improve this, the system sized up and accompanied by a cooling system. It causes an increase in the cost of the mobile communication system itself. On the other hand, heat-generation increases the amount of CO2 in the atmosphere, causing environmental pollution. As a result, much research has been done on power amplifiers, an ultra-high frequency field, to enhance the competitiveness of mobile communication systems, especially efforts to improve efficiency.

However, the implementation method of high-power Power Amplifier has limitations in using Si devices. Compared to Si and GaAs, GaN (Gallium Nitride) semiconductors have advantages in wide band gap (Eg=3.4eV) characteristics and high temperature (700˚C) stability. When used as a power amplifier for mobile network base stations, the power density is more than 10 times higher than conventional Si-based Latterly Diffused Metal Oxide Semiconductor (LDMOS) transistors, reducing power savings by more than 30% compared to radars and satellites. GaN power switching devices for high power have lower switching losses and on-resistance losses than conventional Si-based Insulated Gate Bipolar Transistors (IGBT), which can reduce fuel consumption by more than 10% when applied to hybrid electric vehicles (HEVs) or electric vehicles. [2]

In this paper, we propose a high-efficiency high-power Class-D Power Amplifier with 50W output using GaN elements for the Power Amplifier design with high power.

II. Block Diagram Of Power Amplifier

Figure. 1. shows the Power Amplifier's Block Diagram for transferring power to AC Power to wireless charging receivers. When the transmitter operates in a self-induced manner, the frequency is determined by packet information received from Rx and power is transmitted by receiving PWM frequency input from the power amplifier. In magnetic resonance, it operates at a frequency received from an external crystal oscillator. It uses a structure that can tune PWM signals using Voltage Control Delay Loop (VCDL). It also uses the Deadtime Generator to generate a longer dead time than the turn-off time to prevent possible DC short circuits in the switching moment of the device to prevent current loss. By controlling the Full-Bridge GaN Core via GaN Driver, signal amplification is implemented, and signal amplification can be controlled according to GaN Core's VDD. [1]

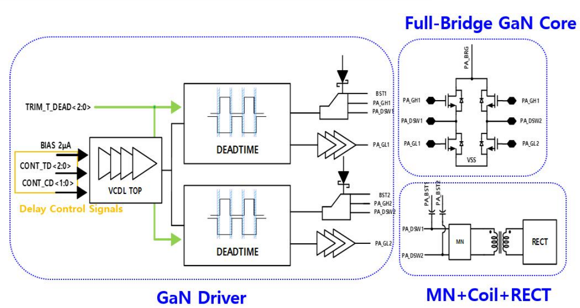

Fig. 1. Power Amplifier Block Diagram

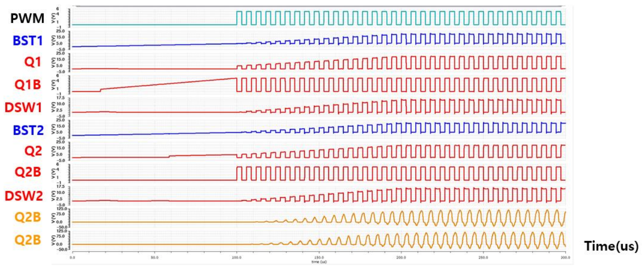

Fig. 2. Top Simulation of Class-D Power Amlifier

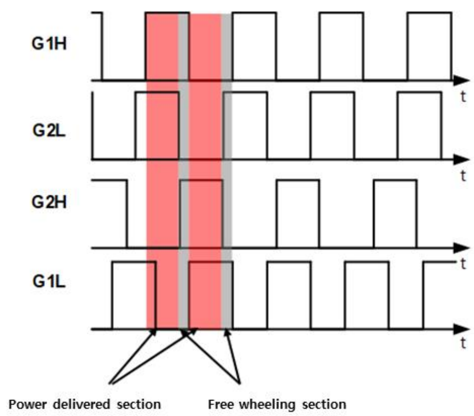

Fig. 3. Timing Diagram for the operation of Power MOS

III. SIMULATION

Figure. 2. shows the simulation results of the proposed Class-D PA. [4] PWM signals can be used by VCDL and Dead Time Generator to output amplified signals using two contradictory signals: High side and Low side. The BST output is amplified through GaN Core. [3]

A. Timing Diagram for the operation of Power MOS

It represents the Timing Diagram for the operation of the Power MOS in Figure. 3. Inside the Power Amplifier from the input frequency, it generates switching signals to drive the Power Amplifier's MOSFET via Delay Cell and Driver. The non-overlap circuit controls the time the MOSFET runs for the Free Wheeling of the Inductor.

B. Simulation result in the magnetic induction scheme of the wireless charge transmitter

Figures 4 and 5 show the Top Simulation resulting waveform in the magnetic induction scheme of a wireless charge transmitter. When the adapter supplied 7V of power and the Power Amplifier's Enable Signal came in, the Power Amplifier operated and the Power MOS' Gate Signal and Switching Node waveforms appeared along the frequency of the magnetic induction method.

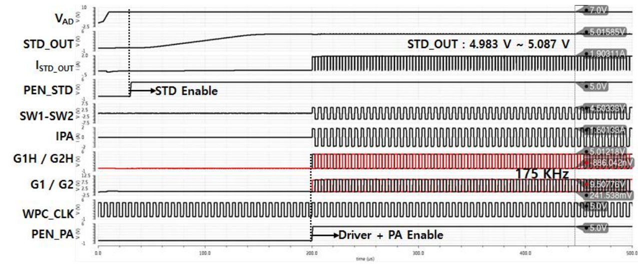

Fig. 4. Simulation of the initial behavior of the wireless charge transmitter.

Fig. 5. Simulation of the steady motion behavior of the wireless charge transmitter.

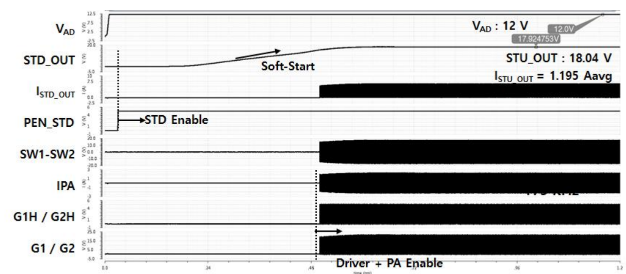

Fig. 6. Simulation of the initial motion of the wireless charge transmitter.

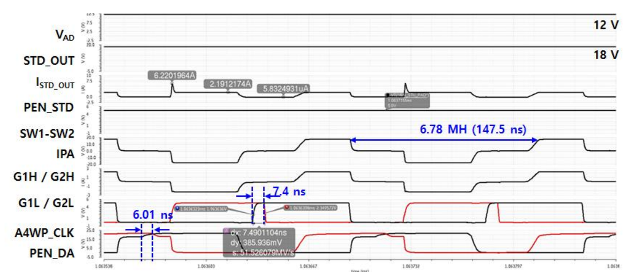

Fig. 7. Simulation of the steady motion of the wireless charge transmitter.

C. Simulation result in the magnetic resistance wireless charge transmitter

Figures 6 and 7 show that the simulation of a magnetic resonance wireless charge transmitter produces a switching voltage at a frequency of 6.78 MHz, resulting in the Power MOSFET operating to produce AC output through switching voltage generation of G1H, G2H, G1L, and G2L.

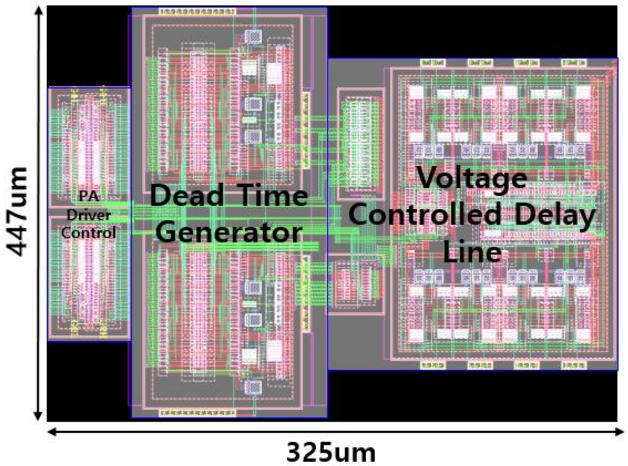

Fig. 8. Layout of Class-D Power Amplifier

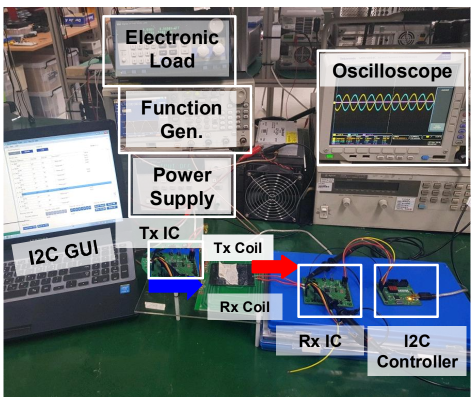

Fig. 9. Measurement environment

IV. The Layout Of Power Amplifier

Figure 8 shows the proposed Top Layout of Class-D Power Amplifier in size 447um × 325um.

V. Measurement Result

Figure 9 shows the measurement environment of magnetic resonance wireless charging. Measurements were using the I2C Controller to control each of IC's registers. To check the efficiency of the integrated system of magnetic resonance, the final system efficiency was determined by multiplying the efficiency of each TX IC and RX IC, and the power consumption also confirmed by adding the power consumption of each IC.

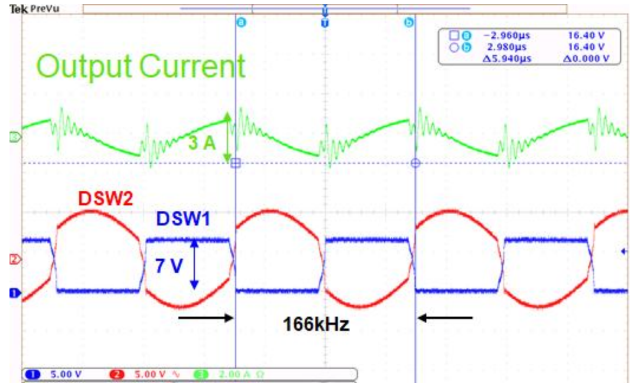

Fig. 10. Wireless charge transmitter behavior (magnetic induction method)

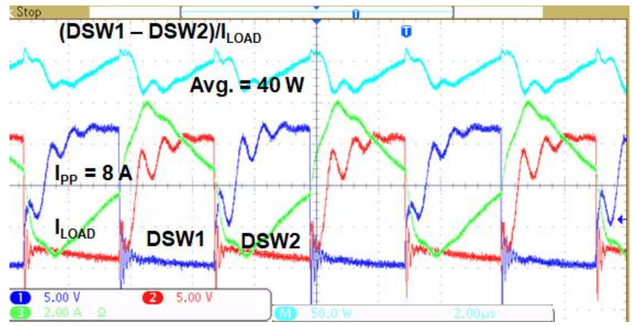

Fig. 11. Wireless charge transmitter behavior (magnetic resonance method)

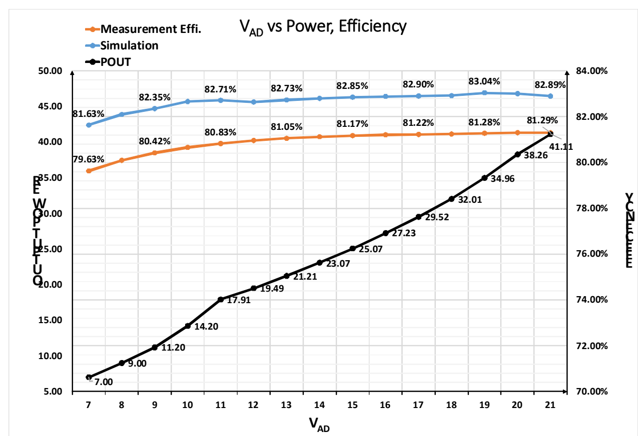

Fig. 12. Output Power and Efficiency Graphs Based on Adapter Voltage

Figures 10 and 11 show the voltage and current on both sides of the coil when operated in magnetic induction/magnetic resonance, respectively, and the interlocking behavior is confirmed by aligning the Rx/Tx coil. In the case of magnetic induction, the error packet is received and the frequency is changed from Digital to Power Amplifier, which changes the error packet by 166 kHz, which controls the power transmission to Rx. For magnetic resonance, an external frequency of 6.78 MHz is applied to generate AC power for the Power Amplifier.

Figure 12 shows the output power and the resulting efficiency changes depending on the voltage VAD supplied to Drain in the High Side Power MOS. It can be seen that output power increases with supply voltage, and efficiency also increases. With dead-time and free-wheeling time at a minimum, we can obtain up to 40 W at a minimum output of 5 W, which confirms that we have achieved our target for the year.

VI. CONCLUSION

GaN (Gallium nitride) semiconductors have more than 10 times the power density of Si-based Latterly Diffused Metal Oxide Semiconductor (LDMOS) transistors used in conventional Power Amplifiers, enabling more than 30% power savings and higher power density and efficiency. If IP is fabricated using GaN, we can obtain larger power for the same size and target for much smaller size with the same power. For the high efficiency of wireless charging transmission and receiving IPs, the On-resistance value had to be low, which required a large area. For high-efficiency, high-power wireless charging IPs, we want to implement differentiated performance IPs by applying Power loss, Power Density, and GaN FET with fast response speed to wireless charging IPs. Compared to conventional Si MOSFETs, GaN FETs have higher speeds, lower costs, and better performance and thermal efficiency than Si, which is around 1000 times higher. In this paper, we propose a differentiated development direction by utilizing/designing a GaN element for wireless charging transmission and reception IP operating at high power/high efficiency of 40W or higher by controlling the full-bridge structure composed of GaN elements using GaN drivers. The proposed Power Amplifier uses the Samsung 180nm process and designs 5 V as supply power.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

REFERENCES

[1] H. Vu, D. Tran and Woojin Choi, "A novel hybrid soft switching full-bridge PWM and full-bridge LLC converter for on-board battery charger applications," 2016 IEEE 8th International Power Electronics and Motion Control Conference.

[2] K. Bathich, A. Z. Markos, and G. Boeck, "A wideband GaN Doherty amplifier with 35% fractional bandwidth," in Proc. 40th Europ. Microwave Conf., pp. 1006-1009, 2010.

[3] H. Nakamizo, K. Mukai, S. Shinjo, H. Gheidi and P. Asbeck, "Over 65% PAE GaN voltage-mode class d power amplifier for 465 MHz operation using bootstrap drive," 2015 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR), 2015, pp. 1-3

[4] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. Elmala, and K. Soumyanath, "A 28.1dBm class-D outphasing power amplifier in 45nm LP digital CMOS," in VLSI Circ. Dig. Tech. Papers, 2009, pp. 206-207.