Design of Voltage Selectable Circuit based on Power Mux for Charger IC

Dae-Geun Cho
Department of Electrical and Computer Engineering
Sungkyunkwan University
Suwon, South Korea
Wkfyddl3tp@skku.edu

Kang-Yoon Lee
Department of Electrical and Computer Engineering
Sungkyunkwan University
Suwon, South Korea
klee@skku.edu

Abstract— This paper proposes Selectable Voltage Genrator. In order to supply a stable power supply voltage, a linear regulator LDO was used. The entire system in which this circuit is used is divided into Charging Mode and Discharging Mode. Charging Mode is the mode to charge the battery with USB voltage (VBUS), and the Discharging Mode is the mode to charge the USB voltage with the battery voltage (VBAT). The input voltage of VBUS is 2.7 ~ 20 V, The input voltage of VBAT supports up to 4 battery cells, The voltage of 1 cell is 4.2 V. According to the suggested input voltage, the voltage supplied into the chip is divided into 5V LDO and 3.3V LDO.

Keywords— High Voltage LDO, Voltage Selectable, Back-to-back Switch, Battery Charger System, Charger IC

I. INTRODUCTION

With the recent advent of the 4th industrial revolution, 'super-connectivity', 'super-intelligence', 'convergence' It is developing into an intelligent society toward the convergence and connection of everything based on the foundation. In particular, AI (Artificial Intelligence),IoT(Internet of Things), Automotive, Big Data Etc. are regarded as key technologies that will lead the 4th industrial revolution [1]. In particular, AI(Artificial Intelligence), IoT(Internet of Things), Automotive, and Big Data are considered as core technologies that will lead the 4th Industrial Revolution. These core technologies are growing based on system semiconductors.

[2] These system semiconductors have functions or control methods suitable for the required system. It is one of the core technologies that will lead the 4th industrial revolution because it has the merit that can be configured. However, when system semiconductors integrate Intellectual Properties (IPs) for System-on-Chip (SoC) that implements a system with various functions as a single chip, they are faced with a limit due to the limited chip area. Accordingly, research on the core design technology of ultra-high speed, low power, and ultra-integrated IP is being concentrated. Recently, with the development of the IoT industry using bio, wearables, portable devices, etc., system industries such as smart cars, smart mobility, smart homes, and smart factories are developing. It is necessary to develop multifunctional SoC products for such smart implementation and low-power SoC products to increase the usage time of mobile smart devices.

In accordance with the diversification of semiconductor chips, a power supply voltage suitable for appropriate use and demand is required. There are also various types of PMIC (Power Management IC), a circuit that manages this voltage. Especially in SoC each, It is important to design a PMIC that meets the specifications and targets required by the application. To improve the power efficiency of these SoCs, various multiple supply voltages and fine-grain point-of-load power management system techniques are used. This is a method of optimizing power efficiency by creating multiple power voltages and supplying appropriate power voltages and currents to various IPs. Multiple regulators are required to create multiple supply voltages. The DC-DC converter switching regulator has good power efficiency, but because it requires an inductor, it has a disadvantage of a large ripple due to chip area and switching. On the other hand, a linear regulator (ex. Low Drop-out Regulator, LDO) has lower power efficiency than a DC-DC converter switching regulator, but has an advantage of relatively small area and small ripple. In order to improve power and area efficiency, one or two DC-DC converter switching regulators are used in the SoC to create a high power-efficient power supply voltage. After that, several power supply voltages are made using several linear regulators with small area and ripple.

II. ARCHITECTURE OF PWR CIRCUIT

Fig. 1 is the structure of the PWR Circuit composed of LDO(Low Drop-out), BGR(Bandgap Reference Voltage Genereator), BGR buffer, Current Bias Generator, UVLO Limiter Circuit, Power MUX, Voltage Select Circuit with back –to back switch . The Power Domain was briefly shown how AVDD, the power supply voltage of the On Chip System side, is generated with VBAT and VBUS voltages. In Charging Mode, the IC operates by generating AVDD by receiving voltage from Micro USB or USB Type-A as VBUS voltage. In Discharging Mode, AVDD is generated by battery voltage.

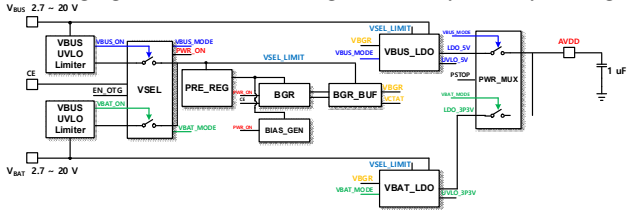


Fig. 1. Diagram of PWR Circuit

At this time, it is designed to automatically select the voltage through the power selector of the charging system.

In the proposed diagram, the VBUS/VBAT UVLO Limiter circuit serves to lower the voltage level of VBUS or VBAT using a Zener diode, and generates VBUS_ON and VBAT_ON Digital (Logically High/Low) signals through UVLO according to VDD voltage without reference voltage.

The VSEL circuit is a circuit that selects VBUS/VBAT power according to the mode among the power generated by the limiter. Here, in order to increase the power efficiency of the circuit, reverse current is reduced by using a back-to-back gate PMOS type Power MUX.

The selected VSEL_LIMIT voltage is used as the power supply voltage of PRE_REG (Pre-Regulator), BGR Buffer, VBUS/VBAT LDO and internal Digital Gate. PRE_REG regulates VSEL_LIMIT voltage of VBUS_LDO to 3V to generate BGR (Bandgap Reference Volatage Generator) and 3V power supply voltage of BIAS_GEN (Current Bias Generator) to give current.

BGR generates VBGR, which is a voltage independent of temperature, and VCTAT voltage, which is inversely proportional to temperature, and these voltages can be driven through the BGR buffer located behind BGR. LDO generates AVDD voltage by regulating VBUS / VBAT voltage to 5V / 3.3V using VBGR voltage as reference voltage. At this time, VBUS/VBAT is a High Voltage Region, and internal Error Amplifier, Bias Generator, etc. operate as VSEL_VLIMIT.

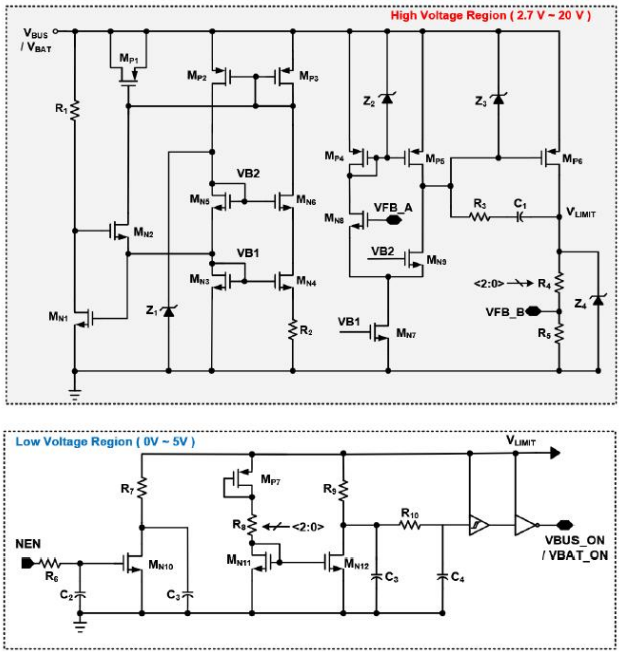
Power By selecting the voltage generated by the LDO through the mux, AVDD, which is the system voltage of the Battery Charger Controller IC, is generated.

III. Design Blocks

A. *VBUS/VBAT UVLO Limiter*

Fig. 2 shows the UVLO Limiter circuit. Reduce the power supply voltage (VBUS/VBAT) to 5V or less to generate VLIMIT voltage. PMOS and NMOS devices in the High Voltage Region are devices that can withstand VDS (or VSD) voltages up to 30V, and VGS can withstand a maximum of 5.5V. A device that can withstand VGS up to 11V was not used because the current mirroring performance was poor compared to the maximum 5V device. MOSFET MP2/3 and MN3/4/5/6 are BMR (Beta-Multiplier) circuits that generate current independent of power supply voltage. MP1, MN1/2, R1 are start-up circuits that enable the BMR circuit to operate. VB1 generated in BMR generates tail current of 5TR Amplifier consisting of MP4/5 and MN8/9, and VB2 is input of 5tr with constant reference voltage. The 5tr Amplifier is negatively feed back to the 5tr Amplifier according to the ratio of R4 and R5 to generate a constant VLIMIT voltage.

Here, the Z1/2/3 Zener diode catches the momentary voltage peak, and the Z4 Zener diode helps the regulation. UVLO operates with the generated VLIMIT voltage as a power source. Table (b) of the figure is the signal specification of the designed UVLO (Under Voltage Lock Out) circuit. UVLO is designed as a circuit that does not need a reference voltage. This circuit is the first circuit of the PWR, and when the level of the power supply voltage (VBUS / VBUS) exceeds a certain voltage, it becomes L to H, and it is designed to satisfy the required spec by giving hysteresis to H to L through Schmitt trigger. Here, by adding the Deglitch operation to R10 and C3/4, the error for power supply noise is reduced. In addition, a trimming bit was added to control the resistance of R4/R8, Operating with External Siganl. And a voltage control function was added accordingly in preparation for variation.



(a)

UVLO Spec	L to H	H to L
VBUS	2.5	2.33
VBAT	2.4	2.23

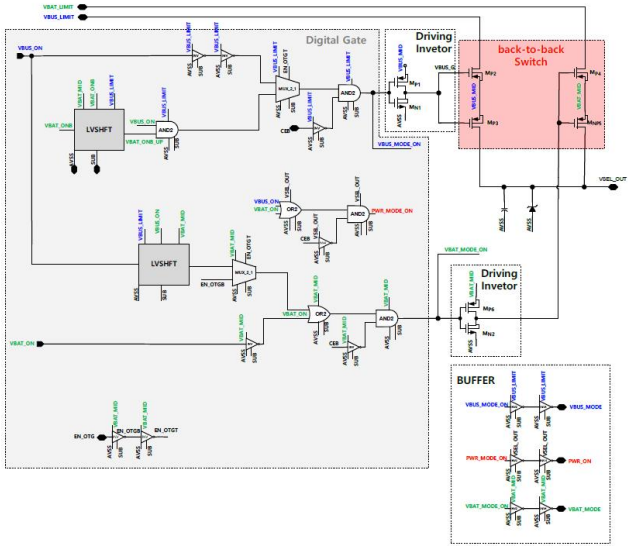
(b)

Fig. 2. Schematic of the UVLO Limiter(High/Low Voltage).

B. *Using a back-to-back switch that generates a mode signal VSEL Circuit*

Fig. 3 shows a block diagram of VSEL Circuit. There are VBUS_LIMIT and VBAT_LIMIT, which lowered the USB power voltage and the power voltage of the battery to the Low Voltage Region, and these voltages are selected as the VSEL_OUT voltage using the back to back switch. The Back-to-back Switch can be used in Bidirectional and Uni-directional depending on the connection direction. In this paper, it was designed with Bidirectionl. Bi-directional back-to-back switch has the advantage of small Reverse Leakage Current in Off state. The MP2/4 used by this switch is The

size of 4mm/50nm and MP4/5 was increased to 8mm/50nm to reduce Ron resistance. By reducing the Ron resistance, the drop voltage was reduced, and at this time, In order to operate a large-sized MOS, the size of the Driving Inverter of MP1/6 and MN1/2 was also optimized.



(a)

Mode	EN_OTG	VBUS_ ON	VBAT_ ON	VBUS_ MODE	VBAT_ MODE	PWR_ON
Charging	L	L	L	L	L	L
	L	L	H	L	1	H
	L	H	L	H	L	H
	L	H	H	H	L	H
Discharging	H	L	L	L	L	L
	H	L	H	L	H	H
	H	H	L	H	L	H
	H	1	H	H	H	H

(b)

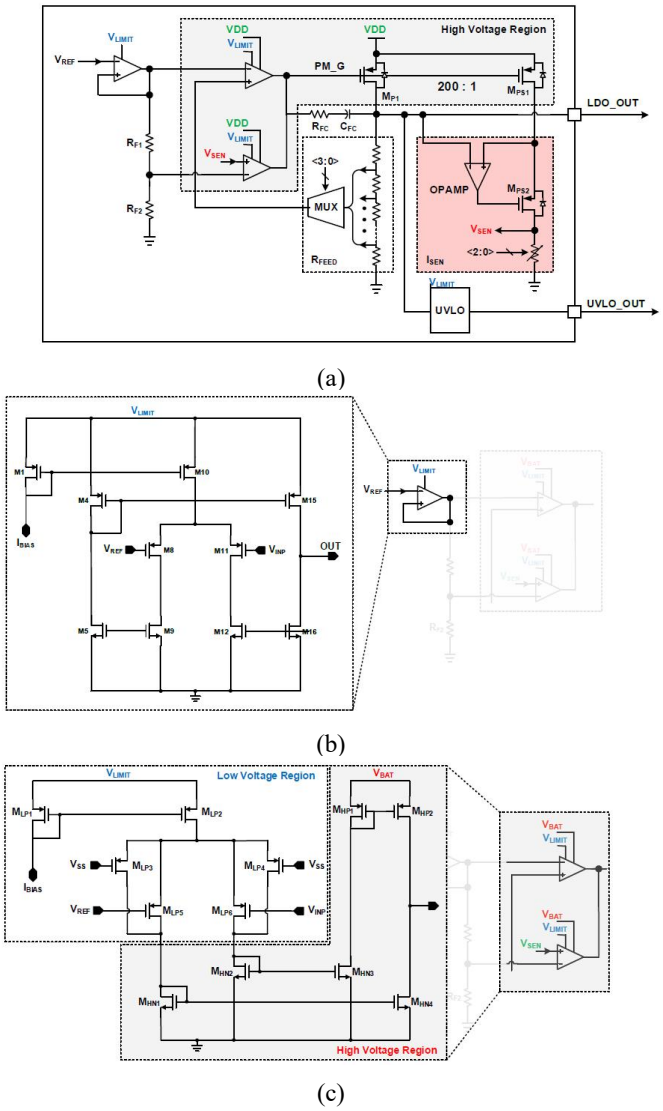
Fig. 3. Schematic of the VSEL Circuit.

Using a digital gate to select with VSEL_OUT voltage, Generates VBUS_MODE_ON, VBAT_MODE_ON, and PWR_MODE_ON signals. VBUS_MODE, VBAT_MODE, PWR_ON signals are generated according to Mode signal EN_OTG received from I2C ,CEB signal received from Pad of Chip and VBUS_ON and VBAT_ON signals generated from the UVLO_Limiter circuit introduced earlier. First CEB(Chip Enable) When “L”, the entire PWR circuit is operated, and when “H”, the entire PWR circuit is turned off. EN_OTG operates as the default “L”, and in this case, it is in Charging Mode. In order to receive the signal of EN_OTG, the entire PWR circuit must be operated and the I2C must be wake-up. Therefore, AVDD is created in the discharging situation that charges USB with battery.

After that, the EN_OTG signal receives “H”. Therefore, since VBAT_MODE becomes H even when EN_OTG is “L”, discharging operation is possible even before I2C wakeup. In addition to this, it is designed to oper ate according to each signal. The core idea of this circuit is power separation using LVSHFT (Level Shifter). The complete logic “H” and “L” implementation was implemented with LVSHFT using only the internal VBAT_LIMIT voltage and VBUS_LIMIT voltage without being supplied with an external constant additional digital logic gate power voltage.

C. LDO based Voltage Generator

Figure 4 is an LDO with a wide voltage range that can operate from 2.7 V to 20 V and an over current protection function added. It is divided into a Low Voltage Region, which is generated from the Limiter and operates with the VLIMIT voltage selected by the VSEL circuit according to the Charging/Discharging Mode, and the High Voltage Region of VBAT or VBUS, which is the power supply voltage.



(a)

(b)

(c)

Fig. 4. Schematic of LDO based Voltage Generator .

The reference voltage of 1.22V with little PVT Variation received from the BGR Buffer was received as the Reference Input Buffer in Figure 4 (b). This input buffer becomes the input of EA, and additionally divides into resistance RF1/2 to become an OCP (Over Current Protection) comparator and plays a role of making a reference voltage. This buffer was designed in an OTA structure.

Figure 4(c) is the LDO's Error Amp and OCP Amp. It is an Amp of PMOS input type because it receives a reference voltage of 1.23V, which is the BGR voltage. It is characterized by dividing the region using VLIMT as the power supply voltage and the region using VDD. By adding a slow start function to MLP3/4, when EA quickly turns on, overshoot of LDO output voltage is prevented.

The operating principle of Over Current Protection is as follows. OCP Amp in Fig. 4(c) is MPS1 with W/L size of 200:1 ratio of MP1 in Fig. 4(a), and current sensing by mirroring 1/200 of load current. When the over current of the load flows by the VSEN signal generated by this current, the OVP Amp operates and increases the gate voltage of the LDO Output Pass transistor. Then, the output voltage decreases, which lowers the load current. Additionally, by adding UVLO to the LDO, when a certain LDO output voltage falls below the specified voltage, a signal that can block the output voltage is generated.In VBUS mode, which is the charging mode, the LDO outputs 5.005V output voltage. Among the VBAT Mode, which is the Discharging Mode, the battery is equivalent to 1 cell.The case was designed as default, and the LDO was designed to output 3.33V output voltage. 5V Mode has been added to RFEED in Fig. 4(a) so that the LDO 5V output voltage can be output when the battery is more than 2 cells.

D. Power MUX

Figure 5 shows the Power MUX circuit proposed in this paper. This is a circuit that selects the voltage of VBUS LDO_5V, VBAT LDO_3.3V (or 5V) according to the Mode Signal generated by VSEL. At this time, PMOS P1/2 used as a switch was designed in the direction of Drain-Source, not a general source-drain connection in consideration of Reverse Current.

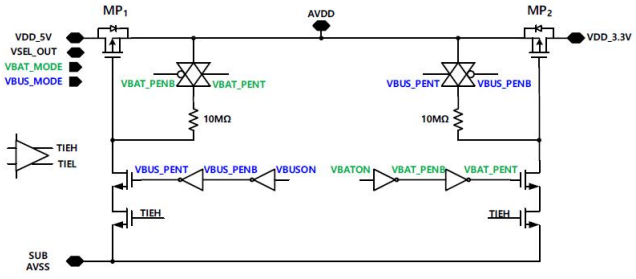
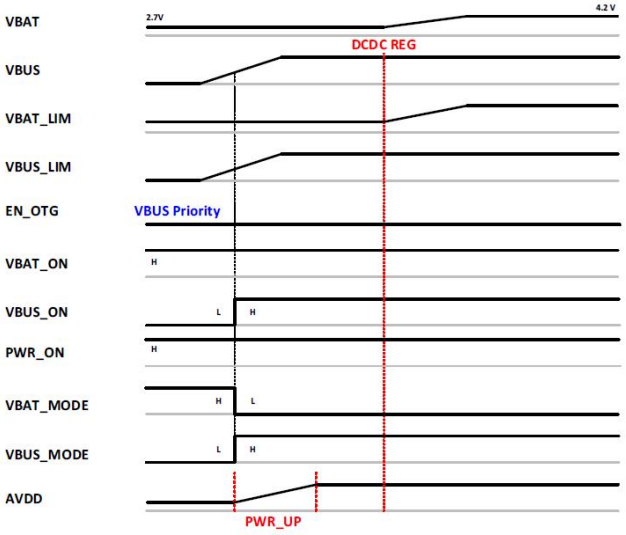


Fig. 5. Schematic of Power MUX. .

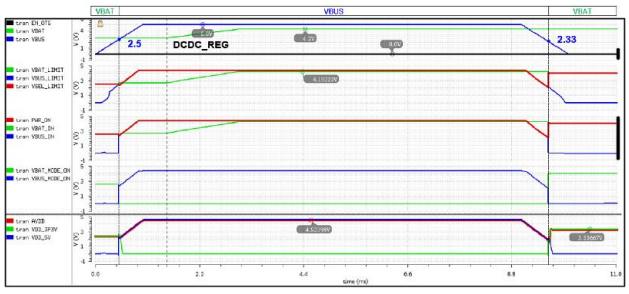
When designing in the drain-source direction, when it is turned off, the diode generated in the drain-source direction blocks the reverse current to prevent the breakdown of the reverse circuit MOS.

IV. Experimental Results

Figure 6 shows Battery 1Cell, Charging Mode Power Sequence and Simulation Result. This mode is to charge VBAT, the battery voltage, with the externally applied VBUS voltage. Since the voltage when VBAT 1 cell is discharged is 2.7 V, the VBAT voltage before charging was modeled as 2.7 V. As VBUS voltage is applied, VBUS_LIMIT voltage increases linearly. The moment the VBUS_LIMIT voltage becomes 2.5 V, the VBUS_ON signal becomes L to H through UVLO. The default of the entire Voltage Generator is Charging Mode, and EN_OTG that determines the mode is L maintain. Therefore, when VBUS_ON becomes L to H, both VBUS_ON and VBAT_ON signals are H, and since they are in Charging Mode, VBAT_MODE becomes H to L, VBUS_MODE becomes L to H, and VBUS LDO 5V operates as VBUS voltage, and 5V voltage of AVDD Is created to become PWR_UP. After the AVDD voltage is generated, the DC-DC Convertor's Control Block operates, and then the DC-DC Convertor's Regulation starts.



(a)

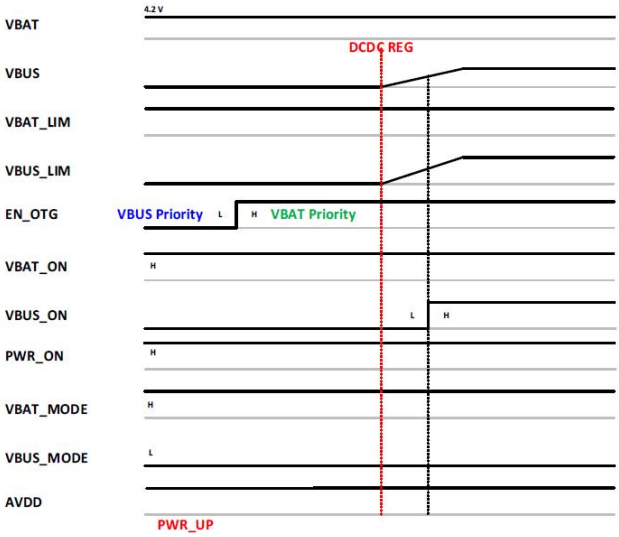


(b)

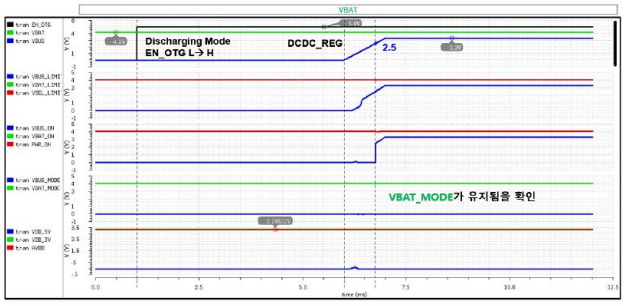
Fig. 6. Charging Mode Power Sequence and Simultion Result.

Accordingly, it can be confirmed that the VBAT voltage is charged. Even if the VBAT voltage is high, As EN_OTG is maintained at L, it can be confirmed that the Charging Mode is also maintained.

Figure 7 shows Battery 1 Cell, Discharging Mode Power Sequence and Simulation Result. Unlike Charging Mode, it is a mode that makes VBUS voltage by discharging the VBAT voltage of the battery. Default is Charging Mode, as mentioned in Case 1. Therefore, as it becomes Discharging Mode, EN_OTG signal should be L to H. EN_OTG signal is a signal received from I2C. 1 Cell Battery's typical voltage is 4.2 V, and AVDD 3.3 V voltage is generated by this voltage. After that, I2C wakes up with AVDD voltage and receives the signal that EN_OTG becomes L to H. After that, the control block of the DC-DC converter operates with the AVDD voltage, and the regulation of the DC-DC converter starts, the VBAT voltage is discharging, and the VBUS voltage is generated. The important point here is, VBUS_ON, When all VBAT_ONs are H, VBAT_MODE should be maintained. Since EN_OTG is maintained at H, it can be confirmed that it operates in Discharging Mode.



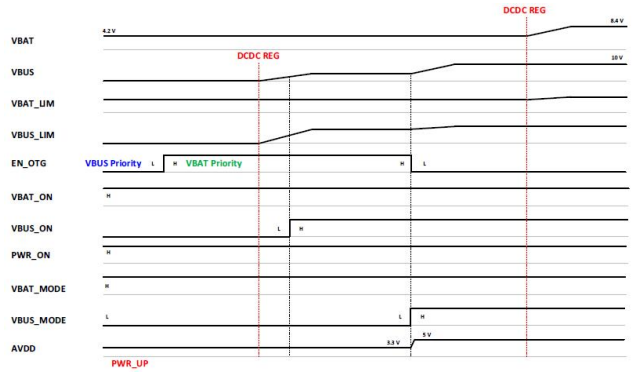
(a)



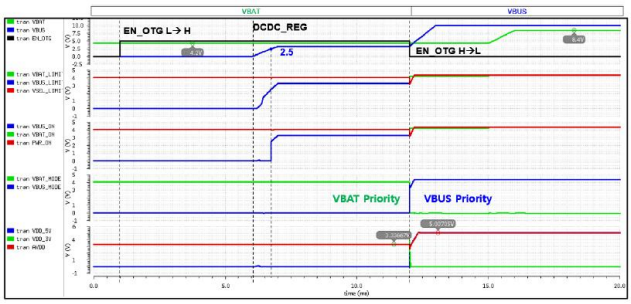
(b)

Fig. 7. Discharging Mode Power Sequence and Simultion Result.

Figure 8 shows Battery 2 Cell, Mode Change Power Sequence and Simulation Result. Fig. 8 is a case of 2 cells, unlike 1 battery cell in Fig. 7, and the VBAT voltage can increase to a maximum of 8.4 V. The initial Discharging Mode operation is the same as in Figure 7. The difference between Fig. 7 and Fig. 8 is the case that changes to Charging Mode through external USB power connection while operating in Discharge Mode. As the USB is connected, PWR_UP is already established and I2C operates, so EN_OTG can give H to L signal. When EN_OTG becomes L, it becomes Charging Mode and becomes VBUS Priority.



(a)



(b)

Fig. 8. Mode Change Power Sequence and Simultion Result.

This has been changed from Discharging Mode to Charging Mode, and both VBUS_ON and VBAT_ON are H, but only VBUS_MODE becomes H. Therefore, it can be confirmed that the DC-DC Convertor operates with VBUS voltage and the 2 Cell Battery is charged up to 8.4 V.

V. Conclusion

In this paper, we designed an LDO based Voltage Generator that automatically selects the power voltage of 2.7 V ~ 20 V to generate the internal power voltage of the DC-DC Controller system. It was used as the power voltage of the internal circuit by lowering the High Voltage to the Low Voltage area through the Limiter circuit, and at this time, it was designed to

automatically select VBUS/VBAT Mode according to the Charging/Discharging Mode through UVLO, which does not require a reference. By using the switch of the VSEL circuit in the Uni-Directional back-to-back method, the Reverse Current could be reduced. By adding an over current protection circuit to the LDO circuit, when an instantaneous load overcurrent flows, the output voltage of the LDO is reduced to add an overcurrent protection operation. In addition, the CTAT voltage generated by the BGR circuit provides an analog signal required for the temperature protection circuit. In the Power Mux that selects the voltage generated by the LDO, the Reverse Leakage Current is reduced by considering the diode in the PMOS drain-source direction. Trimming circuit was added to control voltage and current considering PVT Corner Variation from internal I2C to all circuits. In addition, by adding external CEB and PSTOP signals, the entire Chip Enable and Power Standby Mode can be selected.

Figure 9 shows Top layout of PWR .The LDO based Voltage Generator Circuit proposed in this paper is designed using 0.13um BCD process. The total layout area of PWR Top is 1.2mm X 0.913mm.

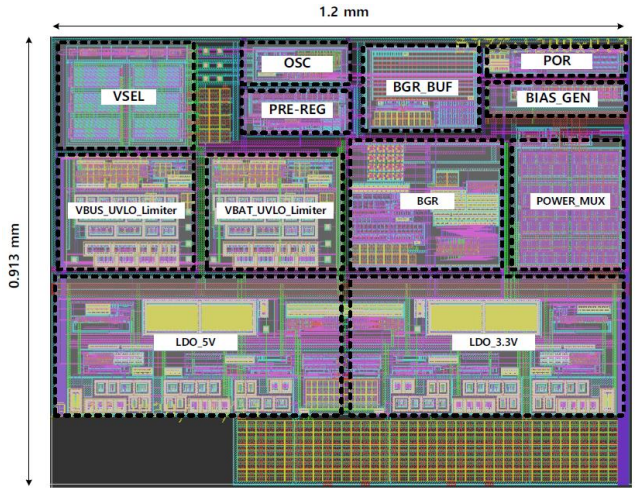


Fig. 9. Top layout of PWR Circuit.

Parameter	Performance Summary(Post simulation)		
	Unit	*[4]*	*This Work*
Technology	nm	130	130
Outout Cap	uF	1	1
Chip-Type	-	On-chip IP	On-chip IP
Drop out Voltage	mV	600	450
Input Voltage	V	2.7~3.6	2.7~20
Quiescent Current	uA	500	147
PSRR	dB	N/A	-76
Load Current	mA	160	250

Parameter	Performance Summary(Post simulation)		
	Unit	*[4]*	*This Work*
Load Regulation	mV/100mA	N/A	5.34

Fig. 10. Performace Summary.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center(IDEC).Korea.

REFERENCES

[1] M. Huang, Y. Lu, S. U and R. P. Martins, "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," IEEE Journal of Solid-State Circuits, vol. 53, no. 1, 20 – 34p, Jan. 2018.

[2] Mohamed El-Nozahi et al., "High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique" IEEE Journal of Solid-State Circuits ,vol. 45, no. 3, pp. 565 – 577, Mar. 2010.

[3] Xiaosen Liu et al., "A Dual-Rail Hybrid Analog/Digital Low Dropout Regulator with Dynamic Current Steering for a Tunable High PSRR and High Efficiency" IEEE Solid-State Circuits Letters(Early Access), Nov. 2020.

[4] Yongwan Park et al.,"High Efficiency Fully Integrated On-Chip Regulatorfor Wide-Range Output Current" 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Oct. 2020.