

# A wideband Single Stage LNA Using a 200-nm GaN HEMT Process

Jiyong Chung

Dept. of Artificial Intelligence Semiconductor Engineering  
Hanyang University  
Seoul, Republic of Korea  
orangecounty@hanyang.ac.kr

Ickhyun Song\*

Dept. of Electronic Engineering Hanyang University  
Seoul, Republic of Korea  
isong@hanyang.ac.kr  
\*Correspondence

**Abstract**—In this paper, we introduce a single-stage wideband low-noise amplifier (LNA) implemented in gallium-nitride (GaN) High-electron-mobility transistor (HEMT) technology. The amplifier operates over the 3–5 GHz frequency range and exhibits  $S_{21}$  of 12.4 dB. To achieve such a wide bandwidth with a single stage, a bandwidth-enhancement technique is employed. By using one capacitor and two inductors in the input matching network with feedback resistor, the proposed design provides improved input matching ( $|S_{11}| < -9$  dB) over a wider bandwidth compared to a single-inductor matching approach. Also, wide output matching ( $|S_{22}| < -10$  dB) is achieved in operation frequency. With a minimum noise figure (NF) of 2 dB and a maximum 1-dB compression point (Output P1dB) of 11.5 dBm and 3<sup>rd</sup> output intercept point (OIP3) of 33.4 dBm, the proposed amplifier offers a clear advantage in chip area compared to wideband LNAs implemented using multiple stages.

**Keywords**—Feedback, GaN, low noise amplifier (LNA), resistive, wideband.

## I. INTRODUCTION

Low-noise amplifiers (LNAs) are among the most critical components in receiver front ends for wireless, communication, and radar systems. A high gain is essential because it suppresses the noise contributions of subsequent stages, and therefore an LNA must be designed to provide sufficiently large gain while maintaining a minimal noise figure. In wideband LNAs, these requirements must be satisfied across the entire operating frequency range.

One widely used technique for realizing wideband operation in LNAs is to cascade several amplifier stages, forming a distributed architecture. In this architecture, the matching network of each stage is intentionally tuned to a different center frequency, generating several distinct gain peaks across the operating band. When these frequency-shifted responses are combined, the individual peaks overlap and merge, resulting in a flattened overall gain that maintains wideband characteristics. While such approaches can deliver wide operating bandwidths and robust RF characteristics, they inevitably require additional matching circuits between stages, resulting in increased chip area, higher dc power consumption, and greater design complexity [1]–[6]. These limitations highlight the growing need for more compact wideband solutions.

An alternative method is to set the input impedance to 50  $\Omega$  by exploiting the transconductance  $g_m$  of a common-gate amplifier. Although this approach can achieve broadband input matching, it demands a substantially large drain load to preserve low-noise performance, thereby adding complexity to the circuit design. In this work, a resistive feedback network is adopted instead, allowing the proposed LNA to achieve wideband characteristics with a simpler structure.

Modern RF systems demand high linearity as well as wideband performance. Gallium-nitride (GaN) high-electron-mobility transistors (HEMTs) are well suited for this purpose due to their low-noise characteristics and excellent power-handling capability with wide energy bandgap (3.4 eV), high breakdown voltage ( $>100$  V), high saturation velocity ( $2.7 \times 10^7$  cm/s) [7]–[9]. These properties allow GaN LNAs to operate without additional filtering or protection circuitry, making them advantageous in terms of reducing overall chip area. In this paper, we present an wideband LNA designed using a GaN HEMT process. The proposed LNA operates over a wide frequency range of 3–5 GHz and, owing to its single-stage architecture, features a simple structure, small chip area, and low noise figure.

## II. GAN HEMT ON SiC SUBSTRATE

The 200-nm gate-length GaN HEMT PDK from WAVICE was used to design the LNA MMIC. This process provides thin-film resistors (TFRs) and metal-insulator-metal (MIM) capacitors, and offers a cutoff frequency ( $f_t$ ) of 50 GHz. The GaN-on-SiC epi structure includes a 2- $\mu$ m Fe-doped buffer layer followed by a 250-Å AlGaIn barrier with an aluminum fraction of 25%. Ohmic contact formation was carried out by implanting  $\text{Si}^+$  ions into the ohmic regions. After performing a shallow recess etch, a Ti/Si/Ni multilayer metallization was deposited to realize low-resistance ohmic contacts. The gate aperture of 0.4  $\mu$ m was patterned by inductively coupled plasma (ICP) etching through the  $\text{SiN}_x$  passivation layer, and a Ni-based metal was subsequently used to form the Schottky gate. Electrical isolation around the device active area was created using  $\text{N}^-$  ion implantation. Finally, a 3- $\mu$ m-thick pad metal incorporating a source-connected field plate was fabricated through gold electroplating [10].

## III. CIRCUIT DESIGN

Fig. 1 shows the simplified schematic of the designed LNA. The LNA was designed as a single-stage amplifier as shown in fig. 1. Wideband power gain and input matching are achieved using the feedback resistor  $R_f$ . The capacitor connected in series with the feedback resistor is used to provide a negative bias to the gate and block dc bias from drain. The small resistor placed in series with the gate is included to improve the stability of the LNA. The value of resistor should be very small like 1  $\Omega$  because thermal noise of resistor at gate can be amplified and lead to degraded noise performance. Inductor  $L_d$  at the drain of  $M_1$  increases the gain at high frequencies while simultaneously forming the output matching network together with  $C_d$ .  $L_{g1}$ ,  $L_{g2}$ , and  $C_d$  constitute the input matching network.  $C_g$  not only forms part of the input matching network but also serves to block the DC bias. The average Q factor of inductor is 18 at center frequency 4 GHz. Compared to multi-stage solutions, the proposed single-stage architecture removes the need for interstage matching

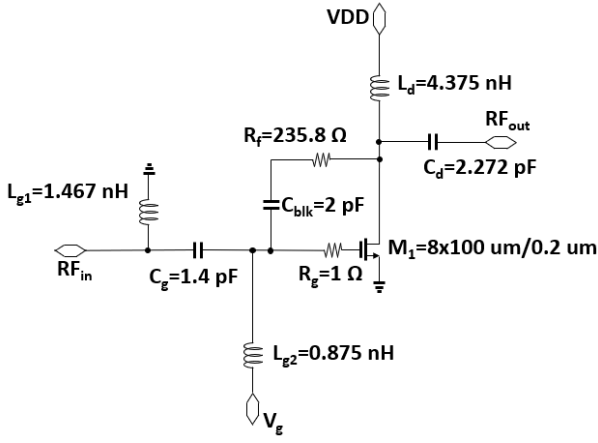


Fig. 1. The simplified schematic of wideband GaN LNA

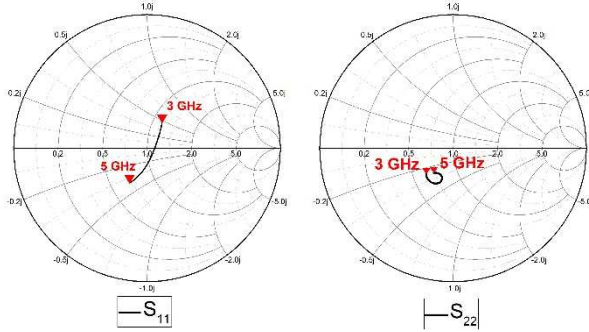


Fig. 2. The smith chart for proposed GaN LNA

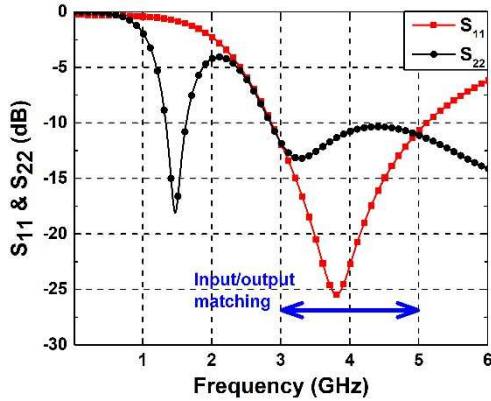


Fig. 3. Input and output return loss of GaN LNA

and reduces cumulative noise contributions, enabling a compact design with competitive performance.

#### IV. SIMULATION

The LNA was designed using the Momentum electromagnetic simulator in Advanced Design System (ADS). It is simulated with a bias condition of  $V_{gs}=-2.2V$  and  $V_{DD}=28V$ . The dc power consumption of the LNA is 1.83 W.

Fig. 2 presents the simulated  $S_{11}$  and  $S_{22}$  characteristics. Although  $S_{11}$  passes through the 50-Ω point, indicating very good matching at the center frequency, the overall matching is not uniformly maintained across the entire band. In contrast,  $S_{22}$  does not intersect the 50-Ω point, so the matching at the center frequency is not as strong; however, the Smith chart trajectories converge toward a localized region within the

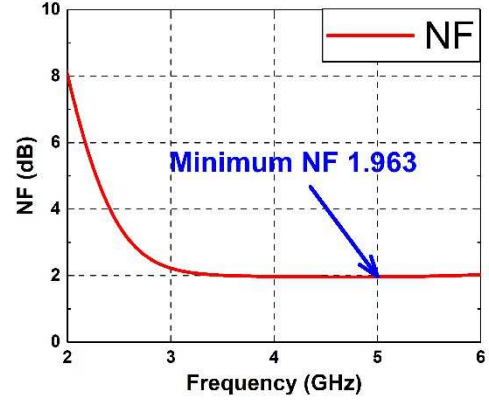


Fig. 4. The NF of proposed GaN LNA

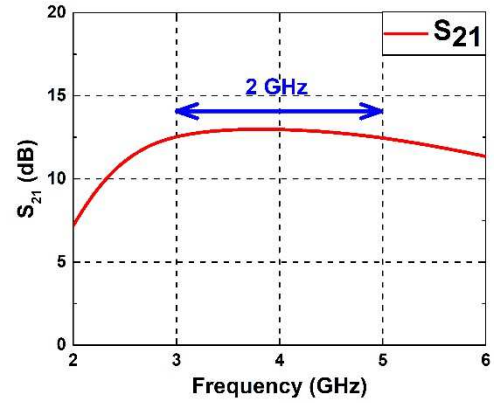


Fig. 5. The gain of proposed LNA

operating band, demonstrating that the output matching is more uniformly distributed over frequency. Using a source degeneration inductor would allow the input matching to become more uniformly distributed across the entire frequency range. However, in this process, the device's source is directly connected to ground through a back-via, which prevents any additional components from being inserted at the source node. Therefore, this approach cannot be implemented in the current design and is planned for investigation in future work.

Fig. 3 presents the simulated  $S_{11}$  and  $S_{22}$  characteristics of the LNA across frequency. The input return loss ( $S_{11}$ ) shows strong matching performance within the 3–5 GHz band, where  $S_{11}$  drops below  $-10$  dB and reaches a minimum of approximately  $-27$  dB near 4 GHz, indicating excellent input matching. The output return loss ( $S_{22}$ ) also remains below  $-10$  dB throughout the same frequency region, confirming stable output matching. These results demonstrate that the designed LNA achieves effective input and output matching over the intended 3–5 GHz operating bandwidth.

Fig. 4 illustrates the simulated noise figure (NF) of the proposed LNA over frequency. The NF rapidly decreases as the frequency increases from 2 GHz and reaches its minimum value of approximately 1.96 dB near 4–5 GHz. Across the intended operating band of 3–5 GHz, the NF remains nearly flat, staying within the low range of about 2–2.1 dB. These results confirm that the LNA maintains excellent noise performance throughout the target wideband frequency range.

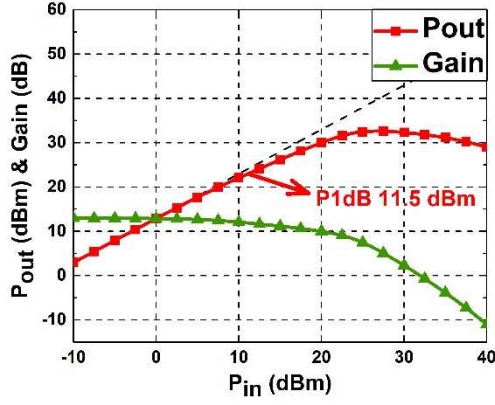


Fig. 6. The P1dB of proposed GaN LNA

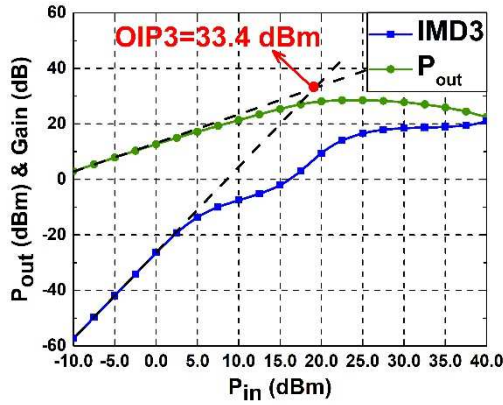


Fig. 7. The OIP3 of proposed GaN LNA

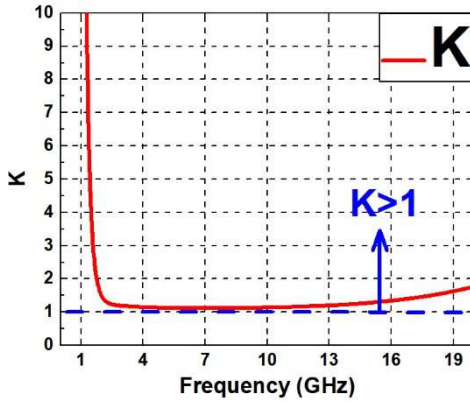


Fig. 8. The K factor of proposed GaN LNA

Fig. 5 shows the simulated power gain ( $S_{21}$ ) of the proposed LNA across frequency. In a wideband LNA, maintaining a flat gain is essential because it ensures uniform amplification across the entire operating frequency range, minimizes signal distortion, and preserves the overall system dynamic range and sensitivity. The amplifier exhibits a maximum gain of approximately 12.4 dB within the 3–5 GHz operating band, where the gain response remains relatively flat. As the frequency increases from 2 GHz, the gain rises to its peak near 3 GHz and then maintains a stable level before gradually decreasing beyond 5 GHz. These results confirm

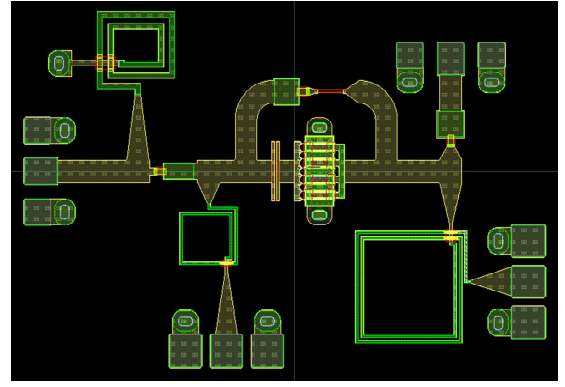


Fig. 9. The layout of proposed GaN LNA

that the LNA provides consistent and sufficient gain across the targeted wideband frequency range.

Fig. 6 presents the 1-dB compression point (P1dB) of the proposed LNA, used to evaluate its linearity performance. To evaluate the P1dB, a single-tone test was performed at the center frequency of 4 GHz. The input power was swept from  $-10$  dBm to 40 dBm during the simulation. As the input power increases, the output power initially follows a linear trend; however, deviation from linearity becomes evident as the amplifier approaches saturation. The P1dB occurs at an input power of approximately 11.5 dBm, where the gain drops by 1 dB from the value. This result indicates that the LNA is capable of handling relatively high input signal levels while maintaining acceptable linearity before compression.

Fig. 7 illustrates the simulated output third-order intercept point (OIP3) of the proposed LNA. To measure the OIP3, a two-tone test was performed. Two input signals were applied at the center frequency of 4 GHz with a frequency offset of  $\pm 1$  MHz, and similar to the single-tone test, the input power was swept from  $-10$  dBm to 40 dBm. As the input power increases, both the fundamental output power and the third-order intermodulation (IMD3) products are plotted to determine the intercept behavior. The extrapolated linear fits of the fundamental and IMD3 responses intersect at an output power level of approximately 33.4 dBm, indicating the OIP3. This high OIP3 value demonstrates that the GaN based LNA exhibits strong linearity and is capable of handling large input signals while minimizing third-order distortion.

Fig. 8 presents the simulated stability factor (K) of the proposed LNA over frequency. The K-factor remains greater than 1 from low frequencies up to nearly 20 GHz, indicating unconditional stability across the entire analysis range. Although the value of K decreases sharply at lower frequencies, it consistently stays above the critical threshold of unity, confirming that no oscillation risk exists within or beyond the intended 3–5 GHz operating band. These results demonstrate that the LNA maintains robust stability over a wide frequency span.

Table III compares the performance of the proposed chip with previously reported designs[7-11]. Although the proposed LNA exhibits a lower gain due to its single-stage implementation, it achieves the smallest chip area among the compared designs. In addition, when compared with other single-stage LNAs, the proposed design occupies a smaller area while offering a wider operating frequency range and

TABLE I. COMPARISON OF OUR WORK AND THE PREVIOUSLY PUBLISHED WIDEBAND LOW-NOISE AMPLIFIER

Ref	Frequency (GHz)	Gain (dB)	Noise figure (dB)	Input return loss (dB)	P1dB (dBm)	OIP3 (dBm)	Chip size (mm <sup>2</sup> )	Process
[7]	4.3-7.4	21.4-24.4	1.47-1.91	9.5-14.8	14.3-20.1	23.3-28.1	2.62	GaN HEMT
[8]	5-6	14	1.3-1.6	12-14.6	22	35	2.55	GaN HEMT
[9]	7.5-11.5	15.3	<1.4	>8.4	9	33	3.77	GaN HEMT
[10]	8-10	25.5	<1.3	>12	-5.4	33.8	4.5	GaN HEMT
[11]	1-6	14	2.9	2.44	N/A	43	N/A	GaN HEMT
This work	3-5	12.4	1.963	>10	11.5	33.4	2.5	GaN HEMT

comparable performance in terms of gain and other key metrics.

## V. DISCUSSION

The proposed LNA adopts a single-stage architecture, which distinguishes it from conventional distributed amplifiers that require multiple cascaded stages along with interstage matching networks. By eliminating these additional matching circuits, the design achieves a substantial reduction in chip area and power consumption. Despite its compact structure, the amplifier maintains a wide 2-GHz operating bandwidth with robust gain and noise performance, demonstrating that single-stage GaN LNAs can achieve wideband operation without the complexity of multi-stage distributed implementations.

Beyond its circuit-level contributions, this work is also relevant to future AI-native RF systems. The proposed single-stage LNA architecture, characterized by reduced structural complexity and a compact design space, is well suited for design automation using AI. Using this topology, AI can learn the characteristic of wideband LNA and design more complex topology based on the information.

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