Machine Learning-Based Optimization of Boosted Voltage in 3T Gain Cell eDRAM

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***Abstract*—This study investigates the impact of boosted read wordline voltage (V_{RWL}) on the read bitline (RBL) voltage swing (ΔV_{RBL}) and read energy consumption in a 3T gain-cell eDRAM implemented in a $65\,\mathrm{nm}$ CMOS process. Circuit-level HSPICE simulations were performed by sweeping V_{RWL} under representative PVT conditions to evaluate the RBL discharge behavior and read efficiency. Increasing V_{RWL} enhances the access-transistor overdrive, thereby increasing ΔV_{RBL} and improving the sensing margin; however, beyond approximately $1.2\,\mathrm{V}$, the discharge improvement begins to saturate while the read energy rises nonlinearly, revealing a clear performance–efficiency trade-off. To quantitatively capture this relationship, a Gaussian Process Regression (GPR)-based machine learning (ML) model was trained using $1{,}000$ simulation samples to predict ΔV_{RBL} and read energy as functions of V_{RWL}. The proposed model achieved mean absolute errors (MAE) of $1.386 \times 10^{-4}\,\mathrm{V}$ for ΔV_{RBL} and $3.27 \times 10^{-19}\,\mathrm{J/bit}$ for energy. Furthermore, an ML-driven weighted-sum optimization identified an optimal boosted voltage around $V_{\mathrm{RWL}} \approx 1.18\,\mathrm{V}$, yielding a predicted ΔV_{RBL} of $0.596\,\mathrm{V}$ and energy consumption of $0.33\,\mathrm{fJ/bit}$. These results demonstrate that the proposed ML-based prediction and optimization framework provides an effective, data-driven voltage design strategy for high-performance gain-cell eDRAMs requiring both fast operation and low power consumption.**

***Index Terms*—embedded Dynamic Random Access Memory (eDRAM), 3T gain cell, Read performance, Energy consumption**

I. Introduction

Today, memory technology plays a key role in diverse fields, including mobile devices, high-performance computing, and artificial intelligence (AI) [1],[2]. Embedded Dynamic Random Access Memory (eDRAM) is attracting attention for its ability to simultaneously achieve high-speed data processing capabilities and high density [3],[4]. In particular, gain-cell eDRAM is considered a promising solution for next-generation systems that require both high-speed operation and low power [5]-[7]. While the conventional 2T gain cell architecture achieves high density and fast read/write operations with a simple cell configuration [8], it suffers from Read Bit Line (RBL) voltage distortion due to interference from unselected cells during read operations, leading to reduced detection accuracy and stability. To address these limitations, the proposed 3T gain cell architecture adds transistors to the read node to isolate the storage node, thereby mitigating the read interference issue [9]. However, the isolated node configuration results in insufficient RBL discharge, resulting in delayed read times and reduced read margins.

In this paper, we propose a method to improve the read path driving capability and the discharge characteristics of the Read Word Line (RWL) by applying a boost voltage to the RWL to address these issues. Furthermore, we propose a framework that automatically searches for the optimal RWL boost voltage by applying machine learning (ML) to simulate data at various boost voltages in addition to the existing simulation-based analysis. The proposed method consists of a training dataset consisting of data from HSPICE simulations performed on a 65nm CMOS process, and a regression-based model quantitatively predicts the trade-off between read performance and energy efficiency. This study presents both the efficiency of high-performance eDRAM design and the possibility of design automation through a data-driven circuit driving optimization approach that utilizes machine learning.

II. 3T Gain Cell

Figure 1 (a) shows the circuit diagram of a 3T Gain Cell eDRAM. Compared to a 2T Gain Cell, the transistor configuration for write operations is identical. However, to address cell interference issues that arise in 2T Gain Cells,

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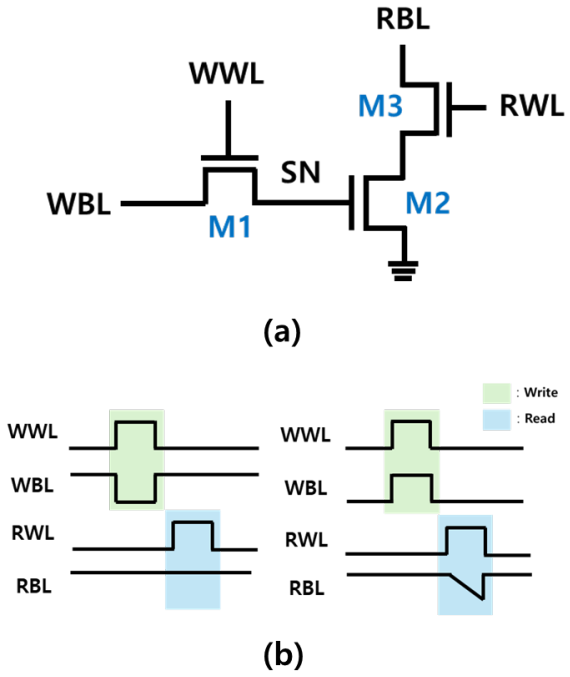

Fig. 1. (a) Schmetic of 3T gain cell and (b) Operation waveform of 3T gain cell

the transistors responsible for read operations are separated into M2 and M3. Figure 1 (b) shows the waveforms for each operation, with the left waveform representing data '0' and the right waveform representing data '1'. The write operation applies a voltage higher than VDD to WWL, strongly turning on M1, which in turn transmits the WBL voltage to the SN. During a read operation, when the RBL is precharged to VDD and the RWL voltage rises from 0 to VDD, M3 turns on. If the voltage stored in SN is 0, M2 turns off, maintaining the RBL voltage at VDD. If SN is 1, M2 also turns on, discharging the RBL voltage. This voltage change is detected by a sense inverter or differential sense amplifier, outputting a 0 or 1. Sufficient discharge of the RBL voltage is necessary for accurate determination, but this can lead to reduced speed due to read node isolation, and in severe cases, RBL voltage sensing failure. While boosting the RWL voltage can improve speed, a high boost voltage can increase energy consumption, making it crucial to determine an appropriate RWL boost voltage.

III. Simulation Results and Discussion

The circuit-level simulations were performed using HSPICE, and Table 1 summarizes the simulation conditions. The TSMC 65-nm CMOS process was adopted under the slow-slow (SS), typical-typical (TT), and fast-fast (FF) process corners. The supply voltage was fixed at 0.9 V, and the operating temperatures were set to 0,° C, 25,° C, and 85,° C. The transistor dimensions (W/L) were 120 nm/60 nm for M1, and 200 nm/60 nm for both M2 and M3. The storage node (SN) was initialized to 0.9 V to represent the read operation

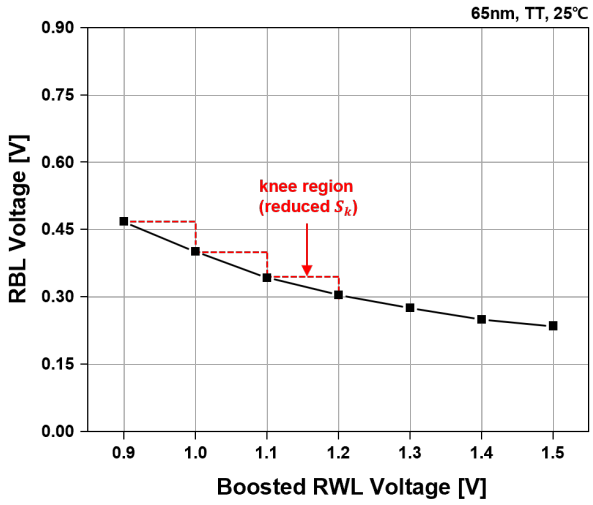

Fig. 2. RBL voltage changes according to boosted RWL voltage

of data '1'. To construct the machine learning dataset, the RBL voltage variation and energy consumption were simulated across different RWL boost voltages under the above PVT conditions. A total of 1,000 data points were collected and used to train the regression-based ML model for predicting optimal RWL boost conditions. This dataset–model integration enables quantitative exploration of the trade-off between read performance and energy efficiency in gain-cell eDRAM.

TABLE I
Simulation Conditions

Parameter	Value
Process	65 nm TSMC
Process Corner	SS, TT, FF
VDD	0.9 V
Temp	0 °C, 25 °C, 85 °C
W/L (M1)	120 nm / 60 nm
W/L (M2)	200 nm / 60 nm
W/L (M3)	200 nm / 60 nm
SN Voltage	0.9 V

A. RBL Voltage

Figure 2 shows the read bit-line (RBL) voltage after applying a boosted read word-line (RWL) voltage for 0.5 ns. As the boosted V_{RWL} increases, the driving capability of the read transistor (M3) is enhanced, which accelerates the RBL discharge and reduces V_{RBL}. However, the reduction in V_{RBL} becomes less pronounced in the higher V_{RWL} region, indicating a diminishing marginal benefit of further boosting. This behavior is consistent with the onset of saturation in M3 and the presence of discharge-limit factors in the read path. To quantify the marginal improvement across each boost interval, the slope S_k is defined as

Equation (1) defines the slope of the RBL voltage drop according to the boosted RWL voltage change.

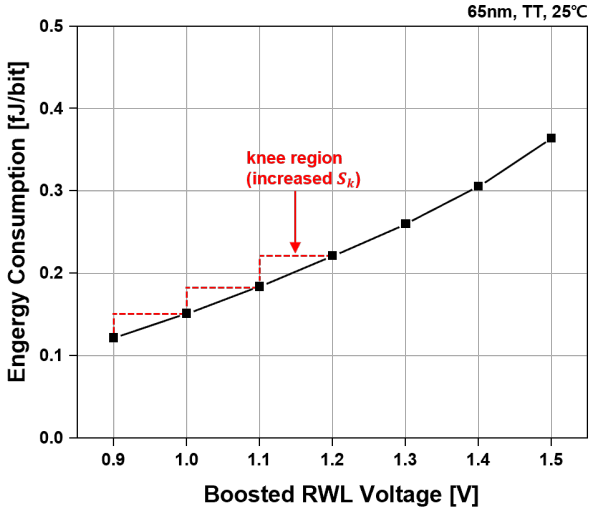

Fig. 3. Energy consumption changes according to according to boosted RWL voltage

$$S_k = \frac{V_{RBL}(V_k) - V_{RBL}(V_k + \triangle V)}{\triangle V}. \quad (1)$$

Here, $\Delta V = 0.1$ V. As highlighted in Fig. 2, S_k becomes noticeably smaller in the 1.1–1.2 V interval, which is marked as the knee region (reduced S_k). Although V_{RBL} continues to decrease beyond 1.2 V, the incremental V_{RBL} reduction per additional V_{RWL} boost is substantially reduced. Therefore, the $V_{RWL} = 1.1$–1.2 V interval is defined as a recommended operating window that captures the transition toward the saturated discharge regime, rather than claiming a global optimum solely from the monotonic trend in Fig. 2.

B. Energy Consumption

Figure 3 shows the read energy consumption as a function of the boosted read word-line (RWL) voltage. As V_{RWL} increases, the dynamic energy required to drive the RWL rises due to charging/discharging of the associated gate and coupling capacitances, and the RBL discharge current through the read path (including M3) generally increases. As a result, the total read energy exhibits a nonlinear increase with V_{RWL}.

To quantify the incremental energy penalty across each boost interval, the local energy sensitivity E_k is defined as

$$E_k = \frac{E(V_k + \Delta V) - E(V_k)}{\Delta V}. \quad (2)$$

Here, $E(V_k)$ denotes the read energy consumption at $V_{RWL} = V_k$, and ΔV is set to 0.1 V. This metric captures the additional energy increase per unit V_{RWL} boost, enabling a quantitative identification of the nonlinearity in the energy–voltage characteristic. As highlighted in Fig. 3, E_k increases noticeably in the 1.1–1.2 V interval, which is marked as the knee region (increased E_k). Beyond this region, further boosting leads to a rapidly increasing energy penalty, which is consistent with the quadratic voltage dependence of capacitive switching energy and the increased read-path conduction loss. Therefore, from an energy-efficiency perspective, the $V_{RWL} = 1.1$–1.2 V interval is selected as a recommended operating window.

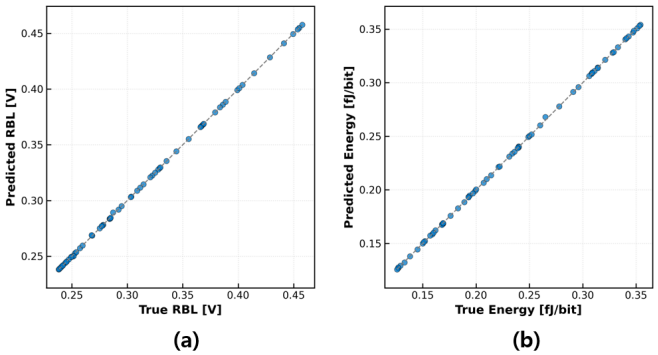

Fig. 4. Comparison between the predicted and actual values obtained from the ML-based regression model. (a) RBL voltage, (b) Energy consumption.

C. ML-based Prediction and Optimization

A machine learning-based prediction model was developed to predict RBL voltage and read energy consumption based on boosted RWL voltage changes. A total of 1,000 simulation data sets were used as training and test data, with the RWL voltage as the input variable and the corresponding RBL voltage and energy consumption as the output variables. The regression model was implemented based on Gaussian Process Regression (GPR) with a Mattern kernel, and all input data were normalized before training. Five-fold cross-validation was performed to prevent overfitting. The model's prediction accuracy was verified by comparison with actual HSPICE simulation results, as shown in Figures 4 (a) and 4 (b). The predicted and actual values showed high agreement, and the mean absolute error (MAE) was very low, at 1.386×10^{-4} V for the RBL voltage and 3.27×10^{-19} J/bit for the energy.

Using an ML model, we performed weighted-sum optimization based on the normalized values of RBL voltage and energy consumption. To find a balance between the two performance metrics, the objective function was defined as Equation (3).

$$J = \alpha \cdot \frac{E}{E_{\max}} - (1 - \alpha) \cdot \frac{\Delta V_{\mathrm{RBL}}}{\Delta V_{\mathrm{RBL,max}}} \quad (3)$$

Here, $\alpha = 0.5$ was set to equally prioritize read speed and energy efficiency. The optimization results revealed an optimal RWL boost voltage around 1.18 V, at which point the predicted RBL voltage swing (ΔV_{RBL}) and energy consumption were 0.586 V and 0.33 fJ/bit, respectively. This coincides with the optimal RWL boost voltage range analytically derived using Equations (1) and (2), demonstrating the reliability and validity of the proposed ML-based optimization model.

IV. Conclusion

In this study, we analyzed the read characteristics of a 65 nm process-based 3T gaincell eDRAM and evaluated the impact of the boosted RWL voltage on the RBL voltage and

energy efficiency. While increasing V_{RWL} improves the RBL voltage discharge rate, a saturation region appears after 1.1–1.2 V, limiting further performance improvement. Furthermore, increasing the boosted voltage also leads to a rapid increase in energy consumption. To address this issue, a GPR-based performance prediction model was developed to quantitatively predict and optimize the RBL voltage and energy consumption as functions of V_{RWL}. The model's prediction accuracy closely matched the actual HSPICE simulation results, and the ML-based weighted-sum optimization yielded an optimal operating voltage that balances read speed and energy efficiency at approximately $V_{\mathrm{RWL}} = 1.18\,\mathrm{V}$. These results are expected to serve as useful guidelines for designing efficient read drive voltages in high-performance memory systems that require fast data access and low latency.

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