Gate-Voltage-Conditioned Leakage-Aware Drain Current Prediction in BCAT Using Support Vector Regression

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***Abstract*—This paper presents a Support Vector Regression (SVR)-based surrogate modeling framework for fast, gate-voltage-conditioned prediction of leakage-aware drain current in a Buried Channel Array Transistor (BCAT). Accurate current estimation under gate-bias sweeps is essential for modern semiconductor design because scaling intensifies strong electric-field effects and leakage-related behavior. Using Synopsys Sentaurus TCAD, we generated 1000 bias-point samples over a gate-voltage sweep range under a fixed drain bias, and used the corresponding drain current as the learning target. With systematic preprocessing and hyperparameter optimization, the trained SVR model achieved a test-set accuracy of $R^2 =$ with RMSE=and MAPE=. Cross-validation further showed stable performance (mean $R^2 =$ with standard deviation). The results confirm that SVR can serve as a highly efficient surrogate model, reducing computational cost by several orders of magnitude compared to TCAD while maintaining physically consistent bias-dependent trends.**

***Index Terms*—BCAT, drain current, leakage current, gate voltage, Support Vector Regression, TCAD simulation, machine learning, surrogate model**

I. Introduction

As semiconductor device dimensions continue to shrink, bias-dependent current behavior—including leakage-relevant operating regions—has become a critical concern for low-power operation, stability, and reliability. In practical evaluation flows, repeated I_D–V_G sweeps under fixed V_D are frequently required for device characterization and device–circuit co-analysis, but TCAD-based sweeps are computationally expensive.

The Buried Channel Array Transistor (BCAT) features a buried conduction path beneath the gate oxide, offering reduced surface scattering and enhanced carrier mobility compared to surface-channel MOSFETs. However, the drain current response to gate bias is strongly nonlinear across subthreshold and inversion regimes, and high-field conditions can emphasize leakage components such as gate-induced drain leakage (GIDL) and tunneling-related behavior. Therefore, a fast and reliable surrogate for predicting I_D as a function of V_G is valuable for accelerating bias exploration and design iteration.

Support Vector Regression (SVR) is attractive for nonlinear regression due to robust generalization and efficiency under limited data—a practical advantage when datasets originate from expensive TCAD runs. In this work, we develop an SVR model to predict BCAT drain current conditioned on the applied gate voltage V_G (with fixed V_D and temperature), targeting rapid and physically consistent I_D prediction across the sweep range.

A. Contributions

The main contributions of this paper are:

- A gate-voltage-conditioned SVR surrogate for BCAT drain current prediction over leakage-relevant bias regions.
- A TCAD-driven dataset construction and a reproducible training pipeline (standardization, outlier filtering, cross-validated hyperparameter tuning).
- Quantitative validation showing $R^2 =$ on the test split and stable cross-validation behavior (mean $R^2 =$).

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II. Theoretical Background

A. BCAT Device and Bias-Dependent Current Behavior

The BCAT structure (Fig. 1) incorporates a conduction channel buried beneath the gate oxide, allowing carriers to flow through a region separated from the Si–SiO_2 interface. As V_G increases, barrier modulation and channel formation drive a rapid transition from subthreshold conduction to strong inversion, producing a highly nonlinear I_D–V_G relationship. Depending on the electric-field distribution and device geometry, leakage-related mechanisms such as GIDL and tunneling components can contribute, especially in off/near-off and high-field regions.

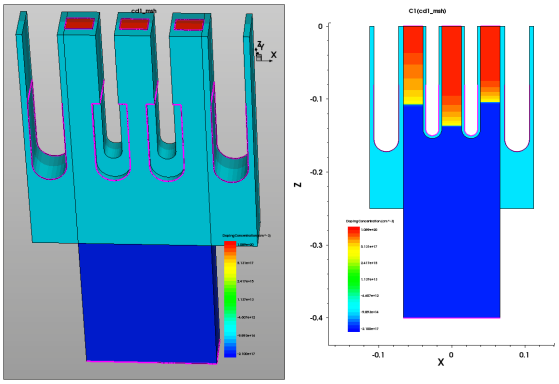

Fig. 1: Schematic of the Buried Channel Array Transistor (BCAT) structure.

B. Principles of Support Vector Regression

SVR extends Support Vector Machines to regression by fitting a function $f(x) = w \cdot x + b$ within an ε-insensitive tube while minimizing model complexity:

$$\min_{w,b,\xi_i,\xi_i^*} \frac{1}{2}\|w\|^2 + C\sum_{i=1}^{n}(\xi_i + \xi_i^*), \tag{1}$$

subject to

$$y_i - (w\cdot x_i + b) \le \varepsilon + \xi_i, \quad (w\cdot x_i + b) - y_i \le \varepsilon + \xi_i^*, \quad \xi_i, \xi_i^* \ge 0.$$

Here, C controls the trade-off between model flatness and tolerance to deviations. To model nonlinearities in the I_D–V_G mapping, we adopt the radial basis function (RBF) kernel:

$$K(x_i, x_j) = \exp\left(-\gamma\|x_i - x_j\|^2\right). \tag{2}$$

III. Methodology

A. Problem Definition

Given a gate voltage input V_G under fixed operating conditions (V_D and temperature fixed), the objective is to predict the corresponding drain current I_D:

$$\hat{I}_D = f(V_G),$$

where $f(\cdot)$ is learned from TCAD-generated pairs (V_G, I_D). This formulation targets fast emulation of TCAD bias sweeps for design-space exploration.

B. Data Generation via TCAD

Device characteristics were simulated using Synopsys Sentaurus TCAD. The BCAT structure was modeled with p-type channel and n-type source/drain regions, and physical models included the drift-diffusion transport model, Shockley–Read–Hall (SRH) recombination, bandgap narrowing, and field-dependent mobility effects. Simulations were performed at 300K.

To construct the learning dataset, the gate voltage V_G was swept within -1.0V to 1.0V while fixing the drain voltage at $V_D = 0.5V$. From the sweep, 1000 bias-point samples were collected and the drain current I_D at each V_G point was used as the prediction target:

$$\text{Input: } [V_G], \quad \text{Output: } [I_D(V_G)].$$

Mesh refinement was applied near the gate–drain overlap region to improve electric-field accuracy and leakage-related current estimation.

C. Data Preprocessing and Model Training

Data were normalized using `StandardScaler` to zero mean and unit variance. Outliers due to numerical instabilities in TCAD were removed using the interquartile range (IQR) method. The dataset was split into 70% training, 15% validation, and 15% testing sets.

Hyperparameters (C, γ, and ε) were optimized via grid search combined with 5-fold cross-validation. The search space is listed (aligned) as:

- $C \in \{0.1, 1, 10, 100\}$
- $\gamma \in \{0.001, 0.01, 0.1, 1\}$
- $\varepsilon \in \{0.01, 0.1, 0.5\}$

Model performance was evaluated using R^2, RMSE, MAE, and MAPE metrics.

IV. Results and Discussion

A. Performance Evaluation Using Scatter Plot

The overall prediction performance is shown in Fig. 2, which compares the SVR-predicted and TCAD-simulated drain currents across the gate-voltage sweep. Each point represents a single TCAD sample, and the diagonal line ($y = x$) denotes perfect prediction.

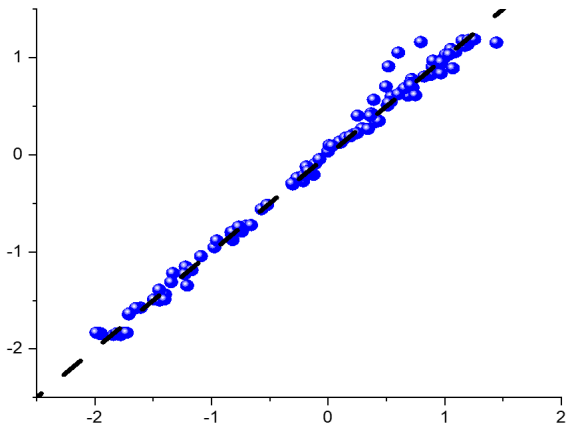

Fig. 2: Scatter plot comparing SVR-predicted and TCAD-simulated drain currents for performance evaluation.

The SVR model achieved R^2 =, RMSE=, MAE=, and MAPE=. Data points are densely clustered near the ideal line, indicating that SVR successfully learns the nonlinear mapping between V_G and I_D. Residuals were centered around zero, suggesting limited systematic bias across the gate-bias range.

B. Physical Consistency and Interpretation

The SVR model exhibits physically consistent bias dependence by reproducing the nonlinear transition of I_D across subthreshold and inversion regimes. In leakage-relevant operating points (e.g., near-off biases), the predicted currents follow the same trend as TCAD, indicating that kernel-based learning effectively encodes the nonlinear dependencies shaped by barrier modulation and electric-field effects.

C. Computational Efficiency

Compared to TCAD, where dense bias sweeps can require substantial runtime, the trained SVR model produces predictions in milliseconds per bias point. This corresponds to an effective speedup of approximately 10^3–10^4 times, enabling integration with optimization algorithms and rapid design-space exploration under varying gate-bias conditions.

D. Cross-validation Analysis and Metric Consistency

To avoid confusion from inconsistent metric reporting, test-split and cross-validation results are reported separately. Across five folds, the cross-validated performance was mean R^2 = with standard deviation , confirming stability and robustness against data partitioning.

V. Conclusion

This study developed an SVR-based surrogate model to predict leakage-aware BCAT drain current as a function of gate voltage under fixed drain bias and temperature. The model achieved high accuracy (R^2 =, RMSE=) and reproduced physically consistent bias-dependent current trends while reducing evaluation time by several orders of magnitude compared to TCAD. Future work will extend the model to multi-input prediction by incorporating additional operating conditions (e.g., V_D, temperature) and structural parameters to further strengthen its contribution to practical device design workflows.

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