Passing Word Line Row Hammering in DRAM via AI-Assisted Pi-BCAT Structure

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***Abstract*—We present a device-level analysis of a passing word-line induced disturbance mechanism in scaled DRAM arrays, referred to as Passing Word Line Row Hammering Effect (PWL RHE). The disturbance is driven by repeated switching of passing word lines in dense cell layouts, which introduces strong electrostatic coupling to adjacent storage nodes. Using TCAD-based transient simulations under representative operating biases with floating storage conditions, we observe pronounced node-voltage excursions during PWL transitions. The disturbance is further amplified by charge trapping/de-trapping in isolation-related interface regions, resulting in node deviations that exceed those of conventional row-hammer conditions by orders of magnitude. To reduce the computational burden associated with long transient cycling, a prediction-guided screening flow is incorporated to pre-select high-risk coupling cases and avoid redundant simulation sweeps. With this accelerated methodology, an enhanced BCAT-based architecture (Pi-BCAT) is shown to significantly suppress PWL-induced node fluctuations compared with a baseline BCAT design, consistent with improved carrier transport control and reduced leakage-sensitive paths. This hybrid framework, combining physics-based TCAD analysis and prediction-assisted exploration, provides a scalable approach for evaluating disturbance-driven degradation and mitigation concepts in next-generation DRAM reliability research.**

***Index Terms*—DRAM , Row Hammering Effect, Passing Word Line Row Hammering Effect, RetentionTime, BCAT**

I. Introduction

Dynamic random-access memory (DRAM) has been continuously scaled to support higher density and higher bandwidth in modern computing systems. A typical DRAM bit-cell is based on a 1-transistor–1-capacitor (1T1C) structure, where a single access transistor connects the storage node to the bitline, and the wordline controls cell access. In scaled arrays, the cell layout is commonly expressed using the minimum feature size, F, and the $6F^2$ cell is widely regarded as the baseline configuration for high-density DRAM products. In a $6F^2$ array, wordlines and bitlines are placed with tight pitch, and adjacent cells share highly compact routing and device spacing. Such compactness improves density, but it also increases parasitic coupling among gates, junctions, and interconnects, which reduces electrical noise margin and makes the stored charge more sensitive to repeated switching activity. As dimensions shrink, reliability margins become tighter, and disturbance-related issues gain importance. Among them, the Row Hammering Effect (RHE) has remained a key concern [1][2][3][4]. RHE is generally associated with repeated wordline activations, which can perturb charge in neighboring cells and, under adverse conditions, lead to sensing errors or data loss. In dense arrays, this disturbance is not only driven by the directly accessed cells but is also affected by "nearby-but-not-selected" lines and nodes. In practice, many cells remain half-selected during repeated operations, and their surrounding lines still experience transitions and capacitive loading. Therefore, even when a target row is not explicitly accessed, nearby switching events can gradually alter the electrical state of adjacent storage nodes. Recent reports suggest that interactions involving Passing Word Lines (PWLs) can further intensify such disturbance behaviors [7][10]. In standard array operation, passing word lines can be repeatedly toggled or experience strong voltage swings while neighboring rows are accessed, which may introduce additional coupling paths into the storage node region. Compared with conventional row-hammer scenarios, PWL-related coupling can create different leakage tendencies and carrier movement behaviors, leading to disturbance signatures that are not well explained by conventional RHE assumptions. This risk is more evident in the $6F^2$ layout because the physical separation between PWL structures and neighboring storage nodes is inherently limited. As scaling proceeds, the effective distance between active gates, isolation boundaries, and storage-node-related regions becomes smaller,

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and the influence of interface- and isolation-related effects becomes more pronounced. Prior studies indicate that repeated switching near sensitive nodes can increase both leakage and node-voltage fluctuation over time, which may degrade sensing stability and reduce data retention robustness [5][10]. While system- and circuit-level mitigations, including error-correcting codes and peripheral design techniques, have been actively explored [6][9], they may not fully address device-level coupling that accumulates gradually through repeated PWL activity and local parasitic interactions [11].A practical challenge is that realistic 3D disturbance simulation is computationally expensive. Meaningful RHE evaluation often requires long activation sequences and repeated cycling, making full TCAD-only sweeps slow and resource-intensive. To improve analysis throughput, prediction-assisted modeling can be used to screen sensitive conditions and focus simulation effort on high-risk cases, reducing redundant runs while maintaining a physics-based interpretation. In this study, we use TCAD transient simulations to evaluate PWL-induced disturbance in terms of cumulative storage-node variation and current-density changes. We then assess a BCAT-based mitigation concept, the Partial Insulator in Buried-Channel Array Transistor (Pi-BCAT) structure [9][10], as a device-level approach to suppress PWL-driven coupling. The results provide a scalable framework to interpret PWL-related disturbance mechanisms in dense $6F^2$ arrays and to guide structural design choices for improved DRAM robustness in future technology generations.

II. Results and Discussion

Passing word-line switching can be a meaningful disturbance source in scaled DRAM arrays because the cell environment is inherently dense and strongly coupled. In a typical $6F^2$-class 1T1C array, wordlines and bitlines are routed at tight pitch, and many "nearby-but-not-selected" conductors still experience large voltage swings during normal operation. As a result, even when a target storage node is not directly accessed, repeated transitions on adjacent control lines can inject or remove charge through parasitic capacitances and field-driven leakage paths. In this context, we evaluate Passing Word Line Row Hammering Effect (PWL RHE) as a coupling-dominant disturbance mode that can accumulate with repeated passing-line activity. To isolate this effect, transient TCAD simulations were configured with a simplified yet representative bias environment. The bitline was held at a fixed operating level, while the passing word line was repeatedly toggled between an OFF bias and an ON bias to emulate periodic switching in a dense array neighborhood. The storage capacitor (and storage node) was initialized to a reference state and maintained in a floating condition so that the node potential could evolve naturally under coupling and leakage, without artificial clamping. The applied waveform followed a basic ramp–hold–ramp profile with short rise/fall transitions and sufficient dwell time at each level to capture both fast capacitive response and slower relaxation components within each cycle. This approach allows direct observation of transient node excursion, recovery behavior after switching, and cycle-to-cycle drift that can build up under repeated stress. The simulated structure reflects a compact array cross-section consistent with a $6F^2$-class environment (Fig. 1). In such a configuration, adjacent cells are placed close to one another, share routing resources such as bitlines, and sit next to passing word lines that run in parallel with minimal spacing. Because of this geometry, the electrical behavior of one line is not fully local; the switching of a passing word line can influence the electrostatic potential distribution around neighboring junctions, isolation regions, and the storage-node vicinity. Two variants were considered: a baseline BCAT-type cell and a modified structure referred to as Pi-BCAT. The Pi-BCAT concept introduces a partial insulating region near the storage-node side, with the intent of weakening undesired coupling and reducing charge loss pathways that become active during repeated line transitions. The stress sequence used in the simulation is summarized in Fig. 2. By repeating identical PWL switching cycles, the simulation captures both the immediate disturbance induced by each transition and the longer-term accumulation trend. The primary monitored quantity is the storage-node potential, since it directly relates to sensing margin and retention stability. In addition, local current-density and potential distributions are examined to identify where charge is being displaced and which regions dominate the incomplete recovery after each switching event.

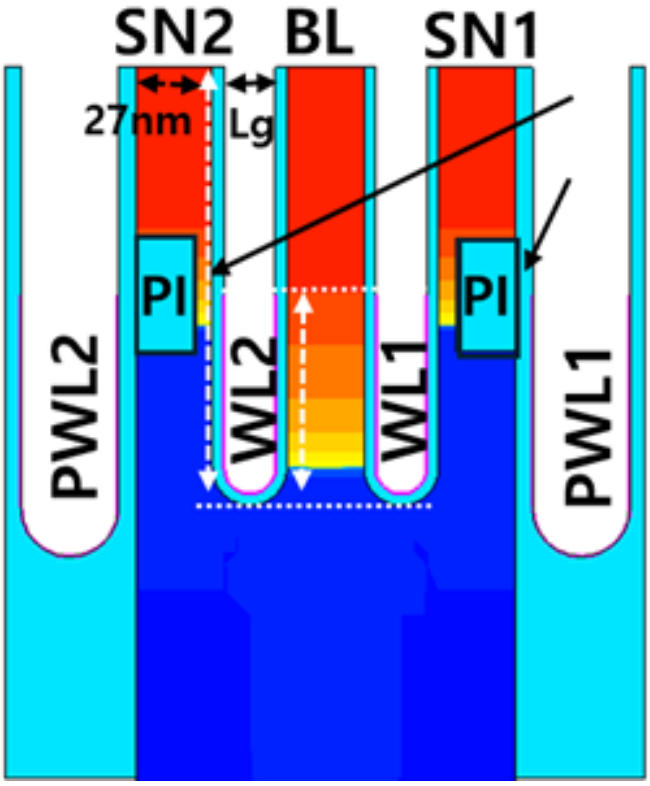

Fig. 1: Cross-sectional schematic of the simulated $6F^2$ DRAM cell showing the BCAT and proposed Pi-BCAT structures. The partial insulator beneath the storage node effectively suppresses leakage and enhances data retention.

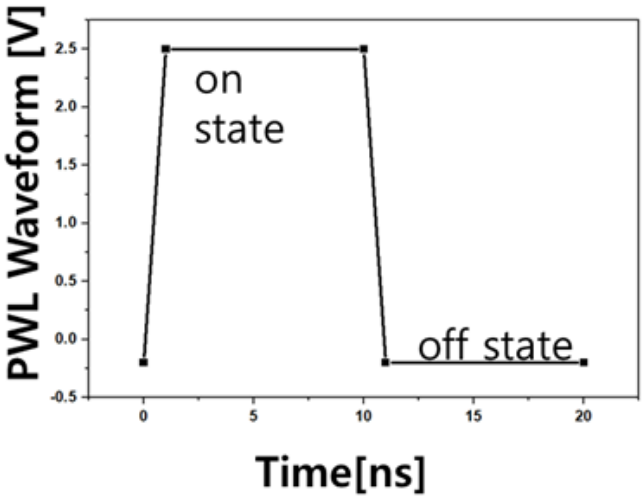

Fig. 2: Applied voltage waveform of the Passing Word Line (PWL) during transient simulation. The bias sequence illustrates ramp-up, ON, and OFF phases used to reproduce Row Hammering conditions.

The underlying mechanism can be explained in terms of field-driven carrier redistribution near isolation-sensitive interfaces (Fig. 3). When the passing word line rises, the local electric field changes rapidly and can pull carriers toward regions adjacent to shallow trench isolation (STI) and other interface-rich boundaries. During the fall and subsequent low phase, not all carriers return to their original distribution. Trapping and de-trapping at interface states, together with local potential gradients and weakly conducting leakage paths, can leave a residual imbalance that appears as an offset in storage-node voltage. Over many repetitions, these small residuals can accumulate, effectively shifting the node baseline and reducing the margin for a stable "0" (or, depending on bias polarity and cell condition, degrading the intended stored state). This interpretation is consistent with the practical observation that disturbance risk is not solely a single-event phenomenon; it is often the result of many transitions where recovery is slightly incomplete. A direct comparison between BCAT and Pi-BCAT under repeated PWL switching is shown in Fig. 4. In the baseline cell, the storage node exhibits a clearer tendency toward cumulative drift with cycling, indicating a stronger coupling/leakage linkage between the passing-line region and the storage-node region. In contrast, the Pi-BCAT structure shows a smaller net shift under the same switching conditions. A plausible explanation is that the added insulating segment increases the effective barrier and reduces the sensitivity of the storage-node region to carrier migration and interface-assisted leakage near the coupling path. In other words, the structural change does not merely reduce the peak transient response; it also improves the recovery behavior, which is critical for suppressing cycle-to-cycle accumulation. To explore the robustness of this mitigation concept, two geometrical design parameters (X and Y), representing the thickness and placement of the partial insulator, were varied across a practical range. However, full 3D transient evaluation across many parameter combinations is computationally expensive because meaningful hammering-like assessment requires long switching sequences to reveal cumulative trends, not only single-cycle responses. For this reason, a hybrid exploration approach can be considered (Fig. 5). In this workflow, TCAD is used to generate a limited set of high-fidelity training traces that capture how the storage-node (or capacitor) voltage changes as switching cycles accumulate. Based on these traces, an AI model could potentially learn the characteristic evolution pattern and then estimate the switching-cycle count needed to reach a predefined disturbance threshold (for example, a node shift level that implies sensing risk). Such a prediction step would not replace physics-based simulation, but it could help screen design candidates and prioritize which bias corners, geometries, or operating conditions warrant full-length TCAD confirmation, thereby reducing redundant long-cycle runs. Overall, this simulation methodology is designed to (i) reproduce passing-line-driven coupling in a compact $6F^2$-class neighborhood, (ii) identify interface- and isolation-related contributors to incomplete recovery and cumulative node drift, and (iii) evaluate whether structural mitigation such as Pi-BCAT can reduce both transient disturbance and long-term accumulation. In addition, the optional integration of prediction-guided exploration suggests a practical path to improve evaluation throughput in cases where exhaustive long-cycle TCAD dominates cost, while still keeping the core interpretation grounded in device physics.

III. Conclusion

This research examined disturbance behavior associated with Passing Word Line (PWL) coupling in scaled DRAM arrays and shows that PWL switching can act as a meaningful contributor to row-hammer-like degradation. Compared with conventional RHE assumptions, the PWL-driven case can produce larger and more persistent storage-node perturbations, including residual effects that may remain after the passing line returns to an inactive state. Such cumulative shifts can gradually reduce sensing margin and retention robustness, increasing the likelihood of disturbance-related failures under aggressive operating conditions. A BCAT-based mitigation concept, Pi-BCAT, was evaluated as a device-level approach to suppress PWL-induced coupling. The results indicate that Pi-BCAT can substantially reduce PWL-driven node fluctuations relative to a baseline BCAT structure, consistent with improved carrier transport control and reduced leakage-sensitive paths. The same structural features also suggest broader benefits against other leakage- and disturbance-related mechanisms that commonly limit reliability in advanced DRAM arrays. In addition to the device-level mitigation, this study highlights the potential role of AI-assisted modeling as a complementary acceleration path. By learning the evolution trend of storage-node (or capacitor) voltage under repeated hammering, a predictive model could be used to estimate the hammer-count

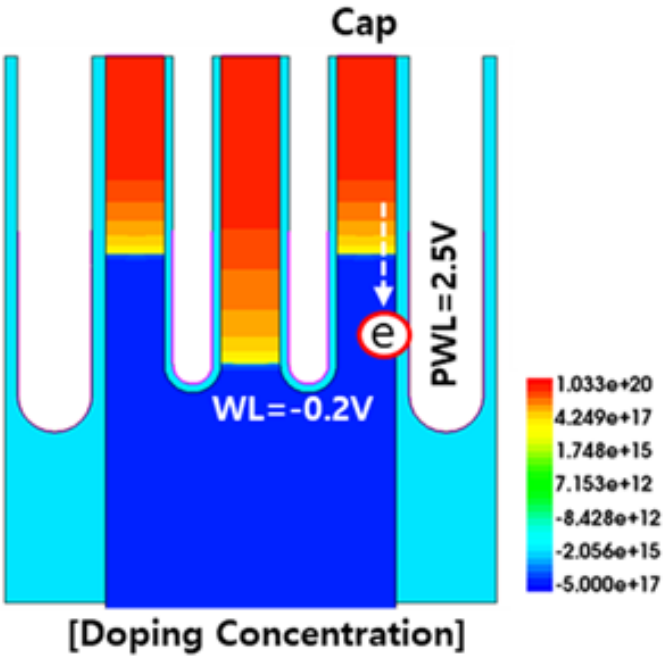

Fig. 3: Mechanism of electron trapping and storage-node voltage rise caused by Passing Word Line transitions. Electrons are temporarily trapped at the STI–Si interface and cannot fully return to the storage node, leading to charge accumulation.

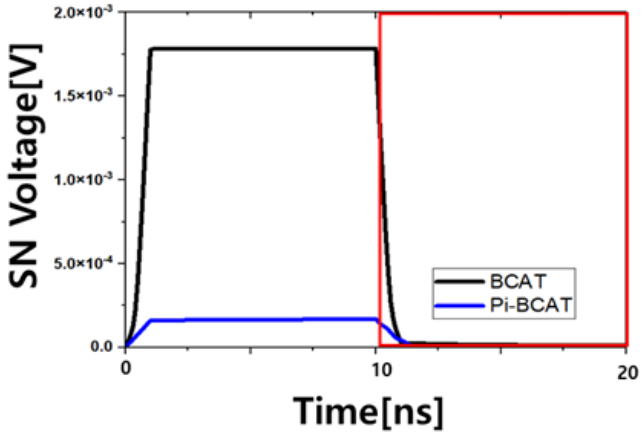

Fig. 4: Comparison of voltage variations between BCAT and Pi-BCAT structures under Passing Word Line hammering. The Pi-BCAT shows approximately 70% lower voltage rise, demonstrating stronger resistance to disturbance.

required to reach a defined disturbance threshold, thereby prioritizing high-risk conditions and reducing the need for exhaustive TCAD cycling in every case. Such a hybrid flow can serve as a practical strategy to improve screening efficiency while maintaining a physics-based anchor through TCAD. Future work will focus on broader operating corners, longer cumulative cycling, and additional structural/process variations to further validate PWL-related disturbance trends

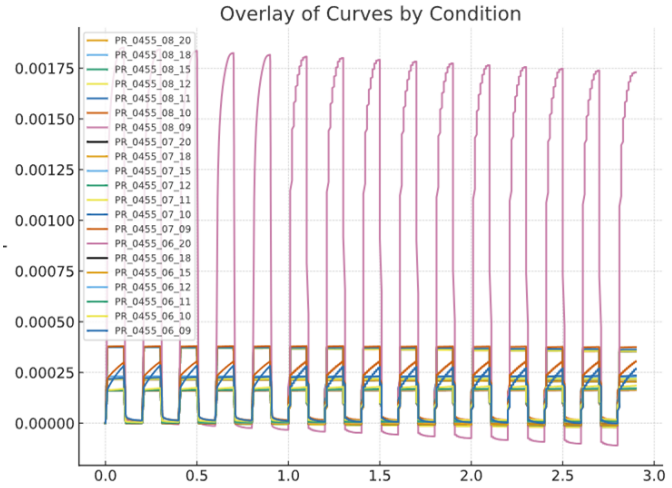

Fig. 5: Pi-BCAT design parameters (X, Y) were explored using a hybrid TCAD–AI workflow. TCAD transient simulations were first used to generate training data that describe how the storage-capacitor (or storage-node) voltage evolves under repeated hammering events. Based on these learned voltage-degradation patterns, an AI model can potentially be used to rapidly estimate the hammer-count required to reach a predefined disturbance threshold (i.e., the onset of hammering-induced failure), thereby reducing the need for full-length TCAD cycling in every case. In this manner, the framework suggests a feasible route to improve screening efficiency and lower computational cost while retaining a physics-based basis from TCAD.

and mitigation effectiveness. Overall, the presented framework—combining device-level analysis, structural mitigation, and the potential of prediction-guided exploration—provides a scalable direction for improving DRAM robustness as technology continues toward tighter geometries and higher integration.

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