SHAP-Based Data-Driven Analysis of an Offset-Canceling Sense Amplifier in DRAMs

Hyerin Lee[1], Geon Kim[1], Dongyeong Kim[1], Suyeon Kim[1], Jewon Park[1],
Shinwook Kim[1], Ryun Kang[1] Sowon Kim[1], Chaehyuk Lim[1], Hyeona Seo[1],
Jeonghyeon Yun[1], Juwon Lee[1], Ujin Choi[2], Eojin Kim[2], Minwoo Jeong[2], and Myoungjin Lee[2,*]
[1]*Dept. of Intelligent Electronics and Computer Engineering, Chonnam National University, Gwangju, South Korea*
[2]*Dept. of Electronics and Computer Engineering, Chonnam National University, Gwangju, South Korea*

lhy2rin@naver.com, rjsdlchd@naver.com, gnodyoung@jnu.ac.kr, bollic4504@gmail.com, you05281@naver.com
sinw1559@naver.com, rkdfbs7535@jnu.ac.kr, kjiwoo8054@naver.com, lch9909@jnu.ac.kr, engine5kor@gmail.com
yunjh0623@naver.com, dlwndnjs2055@naver.com, cuj0528@naver.com, djwls1001@naver.com, blueminw07@naver.com, mjlee@jnu.ac.kr
[*]Corresponding author

***Abstract*—This paper presents an optimization method for the Offset-Canceling Sense Amplifier (OCSA) using a Support Vector Regression (SVR) model. The proposed approach quantitatively analyzes the influence of key design parameters through SHAP (Shapley Additive Explanations) and interprets the trade-off relationships among sensing accuracy, sensing speed, and power efficiency. The analysis results show that structural parameters mainly affect sensing sensitivity and speed, while timing parameters have a dominant impact on stability and power efficiency. Through this quantitative and data-driven analysis, the complex performance characteristics of the offset cancelling circuit are clarified, and a design framework is proposed that enables optimal performance balancing during the design stage.**

***Index Terms*—DRAM, sense amplifier, offset compensation, SHAP analysis, support vector regression, data-driven optimization**

I. Introduction

The sense amplifier (SA) in DRAM is a key circuit that distinguishes stored data by amplifying voltage differences between bitlines [1], [2]. Offset voltage variations caused by process fluctuations in deep submicron technologies directly affect both sensing accuracy and speed. To mitigate these issues, various offset-compensation architectures have been proposed [3]–[10]; however, nonlinear interactions among design parameters under process variation make it difficult to determine an optimal configuration. In particular, complex correlations between structural parameters and timing variables simultaneously influence multiple performance metrics such as decision voltage stability, sensing latency, and power efficiency, making reliable design through empirical adjustment alone challenging.

Previous optimization studies on offset-compensation circuits have primarily focused on average performance or a single evaluation metric, with limited capability to quantitatively reflect parameter correlations or trade-off behaviors. As a result, the balance among critical design aspects such as circuit stability, sensing speed, and power efficiency often remains suboptimal.

To overcome these limitations, this study focuses on a representative offset-compensation architecture, the *Offset-Canceling Sense Amplifier (OCSA)*. An SVR (Support Vector Regression)-based performance prediction model is constructed, and SHAP (Shapley Additive Explanations) is employed to quantitatively evaluate the influence of key design parameters. Through this approach, the relationships among decision voltage ($V_{decision}$), sensing time ($T_{sensing}$), and power consumption ($POWER$) are analyzed, and data-driven optimization guidelines are derived. The proposed framework considers not only individual variable contributions but also interaction effects, enabling systematic adjustment of the trade-offs among accuracy, speed, and power consumption in offset-compensation circuits.

II. Methodology

A. SVR-Based Prediction Model

To capture the nonlinear characteristics of the offset-compensation circuit, a Support Vector Regression (SVR) model was employed. SVR maps the input data into a high-dimensional feature space using a kernel function, allowing effective modeling of nonlinear relationships among design variables. In this work, the Radial Basis Function (RBF) kernel was adopted, and hyperparameter optimization was conducted through a grid search to ensure robust generalization performance. In our previous study, we evaluated multiple regression models across diverse sense-amplifier architectures and confirmed that SVR consistently provides high learning

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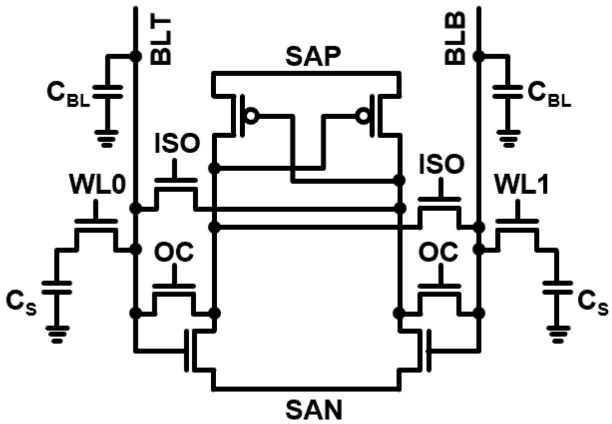

Fig. 1: Schematic diagram of the Offset-Canceling Sense Amplifier (OCSA)

efficiency with robust generalization under limited simulation budgets. Based on this observation, SVR was selected as the primary surrogate model for the proposed OCSA optimization framework.

Simulation data were collected using HSPICE under various design conditions. To reflect the statistical reliability under process-induced offset, we applied Monte Carlo variations of the threshold-voltage mismatch (V_{th}), which dominantly contributes to sense-amplifier offset, at each design point. Accordingly, $V_{decision}$ was not treated as a single deterministic value; instead, its mean and standard deviation were computed across the Monte Carlo samples to directly capture decision variation and stability.

For each configuration, the decision voltage ($V_{decision}$), sensing time ($T_{sensing}$), and power consumption ($POWER$) were extracted. The dataset was divided into 80% for training and 20% for validation, and all input variables were standardized to stabilize the learning process.

The HSPICE simulations were carried out using a commercial 65-nm CMOS process design kit (TSMC). All other circuit parameters not included in the optimization variables were fixed as follows: $V_{CORE} = 0.9$ V, $C_{BL} = 30$ fF, and $C_S = 6$ fF.

B. Input and Output Variable Definition

The overall structure of the Offset-Canceling Sense Amplifier (OCSA) analyzed in this work is shown in Fig. 1. The circuit consists of a conventional latch-type sense amplifier and offset-compensation transistors that compensate for mismatch-induced voltage offsets. The timing of offset compensation is defined by T_{oc} and T_{gap}, while the activation sequence of SAN and SAP nodes is determined by the variable *Type*.

Four key input variables were selected to represent the structural and timing characteristics of the OCSA. The definitions and simulation ranges of these variables are summarized in Table I. Each variable was uniformly sampled within its feasible design range to generate the simulation dataset.

TABLE I: Definitions and ranges of input parameters used for SVR-based OCSA optimization.

Symbol	Description	Range
W_n	Width of nMOS transistor in the sense amplifier	120–380 [nm]
T_{oc}	Duration of offset-compensation phase	0.1–2 [ns]
T_{gap}	Activation interval between SAN and SAP nodes	0–2 [ns]
$Type$	Activation order of SAN and SAP nodes	0 (SAN-first) or 1 (SAP-first)

- The width of the pMOS transistor (W_p) is determined such that the total device width satisfies $W_n + W_p = 500$ nm.

The first variable, W_n, represents the width of the nMOS transistor in the sense amplifier. It determines the driving capability and sensing sensitivity of the circuit. A larger W_n improves sensing speed but increases current consumption, leading to higher power usage. Thus, W_n serves as a structural factor balancing sensitivity and power efficiency.

The second variable, *Type*, denotes the activation sequence between SAN and SAP nodes. This discrete variable (0 or 1) affects the direction of voltage amplification and the initial differential gain during sensing. Different activation sequences alter the symmetry of sensing behavior, influencing both sensing stability and decision accuracy.

The third variable, T_{oc}, represents the offset-compensation time. A longer T_{oc} ensures sufficient offset removal, enhancing stability but resulting in slower sensing and higher energy consumption. Hence, T_{oc} determines the trade-off between sensing accuracy and speed.

The fourth variable, T_{gap}, defines the activation time difference between SAN and SAP nodes. It affects both sensing latency and stability: a larger T_{gap} increases sensing delay, while an excessively small gap causes simultaneous activation, leading to instability. Accordingly, T_{gap} acts as a key timing parameter controlling the precision of circuit operation.

Although the input space is intentionally limited to four variables, the decision stability as well as delay–power characteristics of latch-type sense amplifiers are often governed more sensitively by (i) the effective latch drive strength and (ii) the relative SAN/SAP activation timing, rather than by an equal contribution from all available design knobs. In this context, the selected variables $[W_n, T_{oc}, T_{gap}, Type]$ constitute a compact yet mechanism-oriented design axis that directly captures the dominant structural–timing behavior of OCSA, enabling interpretable analysis of the accuracy–speed–power trade-offs within an efficient design space.

The output variables were defined as the main performance indicators of the OCSA. The decision voltage ($V_{decision}$) reflects sensing accuracy and is evaluated in terms of its mean and standard deviation. The sensing time ($T_{sensing}$) denotes the duration from the start of sensing to the point when the bitline voltage difference reaches the reference threshold (approximately 0.8 V_{CORE}). The power consumption ($POWER$) represents the total energy used during the sensing and offset-

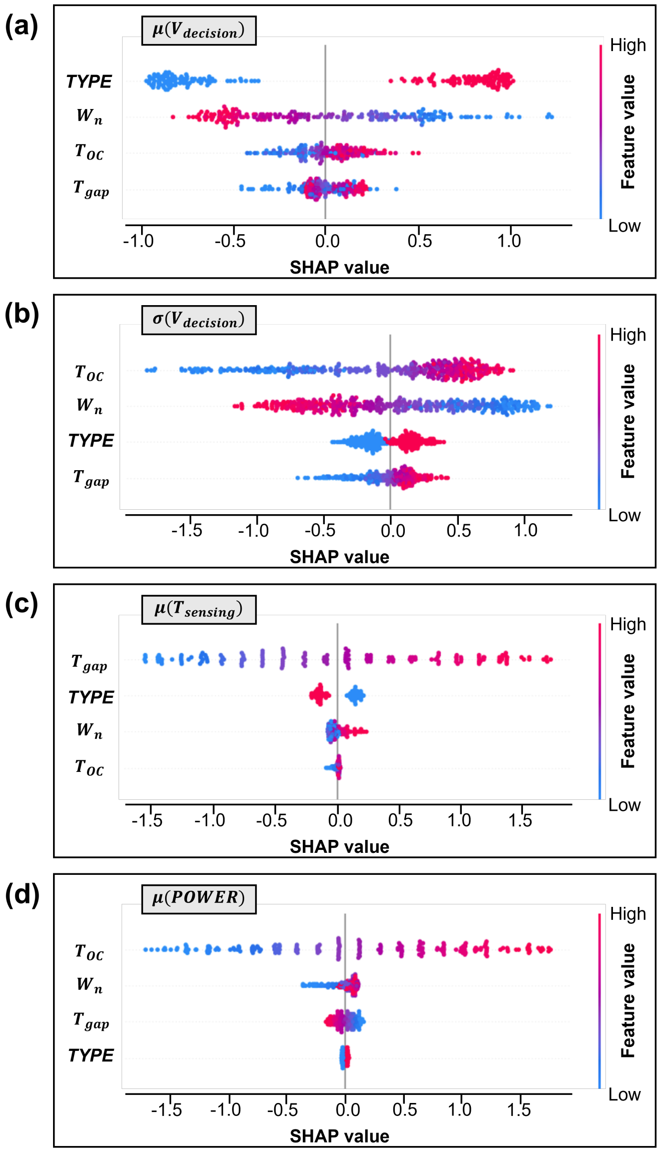

Fig. 2: SHAP summary (beeswarm) plots of the SVR model for (a) mean of $V_{decision}$, (b) standard deviation of $V_{decision}$, (c) mean of $T_{sensing}$, and (d) mean of $POWER$.

compensation process, primarily influenced by T_{oc} and W_n.

These input and output variables collectively capture both structural and electrical characteristics of the OCSA, providing a quantitative basis for analyzing the multi-dimensional trade-offs among performance, speed, and power efficiency.

III. Results and Discussion

SHAP analysis provides both the global influence of the input variables $[W_n, T_{oc}, T_{gap}, Type]$ on each output metric, quantified by the mean absolute SHAP value (mean |SHAP|), and the contribution direction (sign) and distribution visualized through beeswarm plots. Table II summarizes the global importance across the four output metrics, while Fig. 2(a)–Fig. 2(d) present SHAP summary (beeswarm) plots that illustrate how changes in feature values translate into the sign and spread of SHAP contributions for each metric.

TABLE II: Global feature importance summarized by mean absolute SHAP values for each output metric.

Output	$Type$	W_n	T_{oc}	T_{gap}
$\mu(V_{decision})$	0.798	0.436	0.135	0.111
$\sigma(V_{decision})$	0.168	0.531	0.562	0.156
$\mu(T_{sensing})$	0.147	0.058	0.015	0.809
$\mu(POWER)$	0.019	0.088	0.828	0.077

a) $\mu(V_{decision})$: Mean decision voltage: The mean decision voltage $\mu(V_{decision})$ is primarily governed by $Type$ and W_n, whereas the effects of T_{oc} and T_{gap} are comparatively limited (Table II). In Fig. 2(a), higher $Type$ values exhibit predominantly positive SHAP contributions, indicating an association with increased $\mu(V_{decision})$. In contrast, larger W_n values tend to yield negative contributions, suggesting a reduction in $\mu(V_{decision})$. These results imply that the average decision-voltage level is mainly set by the SAN/SAP activation order ($Type$) and the latch drive strength (W_n), while timing variables play a secondary role in shifting the mean level.

b) $\sigma(V_{decision})$: Decision-voltage variation (stability): For $\sigma(V_{decision})$, T_{oc} and W_n show the highest global importance, with $Type$ and T_{gap} acting as auxiliary factors (Table II). As shown in Fig. 2(b), increasing T_{oc} is accompanied by stronger positive SHAP contributions, indicating a tendency to increase $\sigma(V_{decision})$. Conversely, larger W_n values are associated with predominantly negative contributions, implying reduced $\sigma(V_{decision})$. Therefore, from a variation-suppression (stability) perspective, W_n serves as a favorable tuning knob, whereas T_{oc} should be treated as a sensitive variable that requires joint consideration with power-related objectives.

c) $\mu(T_{sensing})$: Mean sensing delay: The mean sensing delay $\mu(T_{sensing})$ is overwhelmingly dominated by T_{gap}, while the contributions of the other variables are minor (Table II). In Fig. 2(c), larger T_{gap} values lead to monotonically increasing positive SHAP contributions, clearly indicating increased sensing delay. Accordingly, T_{gap} functions as the primary design lever for delay reduction, and the remaining variables mainly provide secondary fine-tuning.

d) $\mu(POWER)$: Mean power: The mean power $\mu(POWER)$ is predominantly determined by T_{oc}, whereas the impacts of W_n, T_{gap}, and $Type$ are limited (Table II). In Fig. 2(d), increasing T_{oc} is strongly linked to positive SHAP contributions, leading to higher power consumption. The other variables cluster near zero SHAP values, indicating relatively small effects. Hence, under the considered operating conditions, the power budget is largely dictated by the offset-compensation duration T_{oc}.

e) Integrated interpretation: Role separation and trade-offs: By jointly examining the four output metrics, the functional roles of the design levers and the resulting trade-offs become explicit and are largely separated by metric. While $Type$ efficiently shifts $\mu(V_{decision})$, it does not appear as a dominant factor for delay or power. The structural parameter

W_n is beneficial for reducing $\sigma(V_{decision})$, yet it also tends to decrease $\mu(V_{decision})$, thereby introducing a potential conflict between mean-level targeting and stability improvement. In addition, the timing variables exhibit distinct responsibilities: T_{gap} primarily controls delay, whereas T_{oc} governs power (and contributes significantly to variation). Consequently, tuning priority should be assigned according to the target metric, and in particular, W_n and T_{oc} should be treated as key trade-off levers that require careful balancing during the design stage.

IV. Conclusion

This paper presented a data-driven optimization framework for the Offset-Canceling Sense Amplifier (OCSA) by combining Support Vector Regression (SVR) with SHAP-based interpretability. The SVR surrogate model enables efficient learning of nonlinear performance dependencies observed in sense-amplifier design spaces, and SHAP analysis provides quantitative, metric-specific attribution of key design knobs.

Using Monte Carlo V_{th} mismatch to reflect offset-induced variability, we evaluated both the mean and standard deviation of $V_{decision}$ to directly capture decision stability. The global and local SHAP results show that the dominant design levers differ by metric: the activation order ($Type$) primarily governs $\mu(V_{decision})$, the timing gap (T_{gap}) strongly dictates $\mu(T_{sensing})$, and the offset-compensation duration (T_{oc}) dominates $\mu(POWER)$. In addition, W_n and T_{oc} jointly contribute to $\sigma(V_{decision})$, highlighting a key trade-off axis between stability and cost-related metrics.

Although the input space is limited to four variables, $\{Type, W_n, T_{oc}, T_{gap}\}$ directly represents the mechanism-oriented structural–timing axes that sensitively control latch drive strength and SAN/SAP coordination, enabling interpretable trade-off management within an efficient design space. Future work will expand the design knob set (including device/layout-level factors) and validate the proposed framework with silicon measurements to further strengthen generalization and practical design guidance.

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