Prediction of Trap Behavior under Repetitive Short-Circuit Stress in SiC MOSFETs Using Physics-Informed Gaussian Process Regressions

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***Abstract*—Silicon carbide (SiC) MOSFETs experience high current and electric-field stress during short-circuit (SC) operation, activating interface traps and causing threshold-voltage shifts. This work examines quasi-steady trap behavior under repetitive SC stress using electro-thermal TCAD with an SRH capture/emission model. A 1.2 kV 4H-SiC planar MOSFET was simulated with separate channel and JFET regions containing shallow and deep interface traps. Under repeated SC stress–relaxation cycles, channel traps approach quasi-steady occupancy, leading to a saturating threshold-voltage shift, in line with reported experimental trends. We also propose a physics-informed Gaussian process regression (GPR) that maps single-cycle SC descriptors (pulse energy, peak lattice temperature, and first-cycle threshold-voltage shift) to multi-cycle degradation predictions. The model reconstructs multi-cycle trajectories using only a few calibration cycles per condition, reducing the computational cost of brute-force many-cycle simulations.**

***Index Terms*—4H-SiC MOSFET, Short-Circuit Stress, Threshold-Voltage Shift, Leakage Current, Gaussian Process Regression (GPR), Short-Circuit Ruggedness**

I. Introduction

4H-SiC MOSFETs have attracted significant attention as key switching devices for electric vehicle inverters and high-efficiency power converters due to their wide band gap, high breakdown field, and superior thermal conductivity [1]. However, under Short-Circuit (SC) conditions, a large current and strong electric field are applied within a few microseconds, causing thermal and electrical degradation at the gate oxide and SiC/SiO_2 interface. During this process, interface traps capture and emit carriers, leading to threshold voltage shifts (ΔV_{th}) and potential changes in leakage current. These degradation mechanisms are recognized as key factors limiting SC robustness. Maresca et al. [2] identified spatially non-uniform trap distributions and showed that TCAD models incorporating this non-uniformity can better reproduce current–voltage characteristics. Meng et al. [3] experimentally investigated repetitive SC stress and found that channel and JFET regions exhibit distinct trap characteristics with different impacts on device degradation. Physics-informed machine learning has been applied to power MOSFET prognostics, primarily under thermal cycling conditions [4]. These approaches typically use ON-state resistance as a failure precursor and embed physical constraints—such as monotonic degradation trends—into data-driven models, improving prediction accuracy and interpretability with limited training data. However, most existing studies focus on package-level failures such as die-attach delamination, and few have addressed gate-oxide or interface-trap degradation. Moreover, the application of such approaches to predict trap-induced degradation under repetitive short-circuit stress remains largely unexplored. In this work, we examine SRH-driven quasi-steady trap occupancy and threshold-voltage behavior in 4H-SiC MOSFETs under repetitive SC stress using TCAD simulations. Shallow and deep interface traps were implemented in the channel and JFET regions, respectively. Furthermore, we employ a physics-informed Gaussian process regression (GPR) that uses single-cycle descriptors—SC pulse energy (E_{SC}), and first-cycle threshold-voltage shift ($\Delta V_{\text{th}}(1)$)—to predict multi-cycle degradation parameters obtained by curve fitting, enabling trajectory reconstruction with quantified uncertainty [5].

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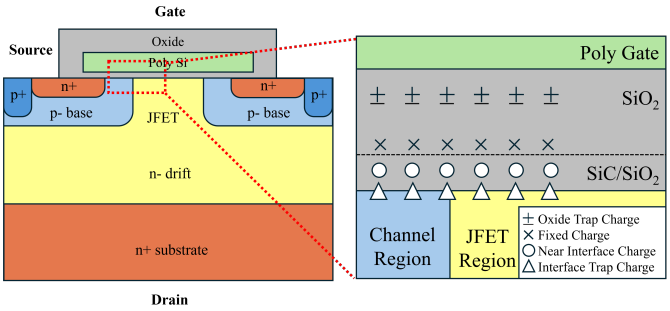


Fig. 1. Schematic illustration of the simulated 4H-SiC planar MOSFET structure (left) and interface trap distribution at the SiC/SiO_2 interface (right). Different trap types are shown: oxide trap charge (±), fixed charge (×), near-interface charge (○), and interface trap charge (△).

II. TCAD Simulation and GPR

Short-circuit (SC) stress was simulated using the Sentaurus TCAD to examine trap dynamics and threshold-voltage shift in a 1.2-kV 4H-SiC planar MOSFET. A physics-informed GPR framework is also introduced, which uses single-cycle descriptors from these simulations to predict multi-cycle degradation trajectories.

A. Device Structure

The simulated device adopts a half-cell geometry of a commercial 1.2-kV 4H-SiC planar MOSFET (Wolfspeed C2M0080120D) [6] as the reference structure for TCAD calibration. Fig.1 shows the simulated device structure (left) and charge states at the SiC/SiO_2 interface (right). Following Maresca et al. [2], the interface was divided into two regions—one above the channel and the other above the JFET—each assigned distinct trap distributions to represent the experimentally observed non-uniform interface properties. The channel region contains acceptor-type traps near the conduction band, which capture electrons and cause threshold-voltage shifts. The JFET region includes both acceptor and donor traps that influence leakage current paths.

B. Physical Models

The Sentaurus TCAD framework was configured with physical models appropriate for SiC device simulation. Carrier mobility followed the Lombardi model with surface roughness and phonon scattering terms. Self-heating was solved with electro-thermal coupling to capture transient temperature rise during short-circuit stress. Interface trap dynamics were modeled using the Shockley–Read–Hall (SRH) formalism with temperature dependent capture cross sections.

C. Simulation Conditions

TCAD mixed-mode simulations were used to emulate short-circuit stress. A gate voltage of $V_{GS} = -5/20$ V and a drain voltage of $V_{DS} = 600$ V were applied, corresponding to 50% of the rated blocking voltage. For each condition, 1–10 SC cycles were simulated at two ambient temperatures: 25 °C, 150 °C. The threshold-voltage shift ΔV_{th} was extracted from

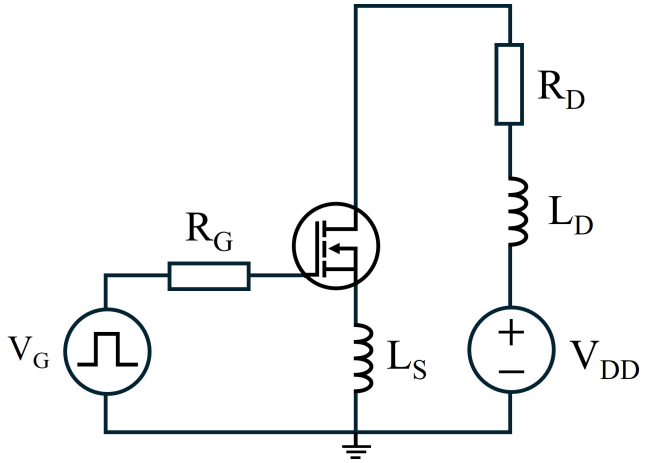


Fig. 2. Circuit diagram for TCAD Mixed-Mode Short-circuit test.

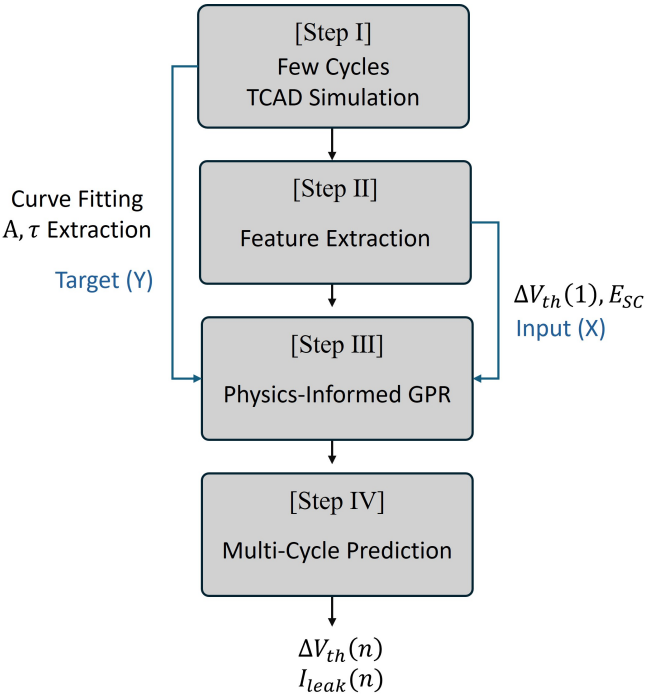


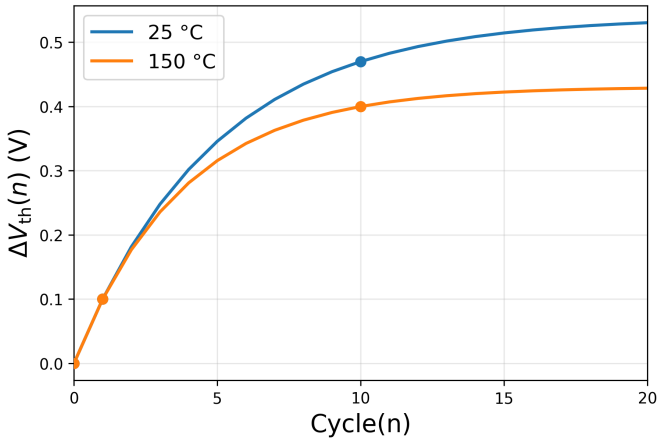
Fig. 3. Flowchart of the GPR-based prediction.

I_D–V_G curves at $V_{DS} = 20$ V after each cycle. Fig. 2 shows the circuit configuration used for the SC stress simulation, with $R_G = 7\ \Omega$, $R_D = 10$ mΩ, $L_S = 5$ nH and $L_D = 10$ nH.

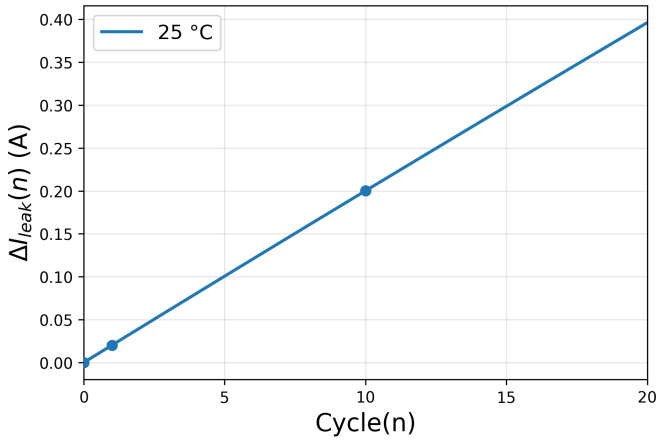
D. Physics-Informed GPR

Fig. 3 illustrates the proposed prediction process. A physics-informed Gaussian process regression (GPR) is employed to predict multi-cycle degradation from first-cycle features.

From the first SC cycle, input features $\mathbf{X}$ are extracted: the SC pulse energy $E_{SC} = \int_0^{t_{SC}} V_{DS}(t) I_D(t)\, dt$, the first-cycle threshold-voltage shift $\Delta V_{th}^{(1)}$, and the ambient temperature T_{amb}.



(a)



(b)

Fig. 4. GPR-based multi-cycle predictions under SC stress:(a) threshold-voltage shift versus cycle, and drain leakage currentversus cycle.

The multi-cycle evolution of the threshold-voltage shift is assumed to follow a monotone saturating form, reflecting the gradual occupation of available trap states:

$$\Delta V_{\text{th}}(n) \approx A\left(1 - e^{-n/\tau}\right), \tag{1}$$

where A (V) denotes the asymptotic shift and τ (cycles) the time constant (approximately 63% of A at $n = \tau$ and about 95% by $n \approx 3\tau$). The target parameters $\mathbf{Y} = \{A, \tau\}$ are obtained by fitting this model to the few-cycle TCAD data (3–8 cycles per condition).

A standard GPR then maps the input features $\mathbf{X}$ to the target parameters $\mathbf{Y}$, reducing the need for computationally expensive multi-cycle TCAD simulations.

III. Results and Discussion

Fig. 4 shows the multi-cycle prediction results generated by the physics-informed GPR using first-cycle features. Fig. 4(a) shows the threshold-voltage shift $\Delta V_{\text{th}}(n)$ versus cycle index n, and Fig. 4(b) shows the drain leakage current $I_{\text{leak}}(n)$ versus n. Solid lines denote the fitted saturating curves, and markers indicate TCAD data points. At 25 °C, the fitted parameters are $A = 0.539$ V and $\tau = 4.88$ cycles, while at 150 °C, $A = 0.431$ V and $\tau = 3.78$ cycles (Fig. 4(a)). Higher temperatures lead to faster saturation, consistent with enhanced trap capture rates at elevated temperatures. The leakage current $I_{\text{leak}}(n)$ also increases with cycle count, reflecting trap-assisted tunneling in the JFET region as reported in prior studies [3].

IV. Conclusion

This paper presents a physics-informed GPR approach to predict trap-induced threshold-voltage shift in 4H-SiC MOSFETs under repetitive short-circuit (SC) stress. Using first-cycle features—SC pulse energy, ambient temperature, and first-cycle threshold-voltage shift—the model estimates the asymptotic degradation level A and time constant τ, reconstructing the multi-cycle degradation trajectory from limited TCAD data. The proposed approach reduces the computational cost of multi-cycle TCAD simulations while capturing the saturating degradation behavior. Limitations include reliance on a single device structure and limited stress conditions, which may constrain generalization. Future work will validate the approach with experimental measurements and extend it to broader operating conditions.

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