Deep Learning-Based Pareto Optimization Framework for LDMOS Transistors

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***Abstract*—Laterally Diffused Metal-Oxide Semiconductor (LDMOS) devices are crucial for high-power and high-frequency applications, but their optimization requires balancing complex trade-offs among structural parameters that determine breakdown voltage (BV), on-resistance (R_{on}), and gate–drain charge (Q_{gd}). Conventional single-objective approaches often fail to identify globally optimal solutions across competing performance metrics. This study presents a deep learning-based surrogate modeling framework integrated with multi-objective Pareto optimization for efficient LDMOS design. A ResNet-1D architecture trained on TCAD simulation data accurately predicts electrical characteristics from five key parameters (L_1, N_1, T, N_{PWELL}, N_{SUB}), ..., achieving $R^2 > 0.99$ while reducing computational cost by up to 53.3× compared with TCAD (Table I). SHAP analysis revealed that BV is most sensitive to drift thickness (T) through RESURF effects, while R_{on} and Q_{gd} are primarily controlled by channel doping (N_1). Pareto optimization between BFOM (BV^2/R_{on}) and SFOM ($Q_{gd} \times R_{on}$) quantified the inherent trade-off between conduction efficiency and switching loss, enabling systematic identification of application-specific optimal designs. The proposed framework provides a computationally efficient and physically interpretable platform for LDMOS optimization, facilitating rapid design space exploration and goal-aware device engineering for power semiconductor applications.**

***Index Terms*—LDMOS, surrogate modeling, deep learning, SHAP, Pareto optimization**

I. Introduction

LDMOS (Laterally Diffused Metal-Oxide Semiconductor) devices are widely utilized in high-power and high-frequency application fields such as switching power converters, wireless transmission amplifiers, and automotive electronic systems, due to their structure that can simultaneously secure high breakdown voltage and excellent power efficiency. In particular, LDMOS has attracted attention as a leading platform for silicon-based high-power device technology because it is based on a lateral structure, offering high compatibility with integrated circuit processes and enabling cost-effective process implementation [1], [2], [3].

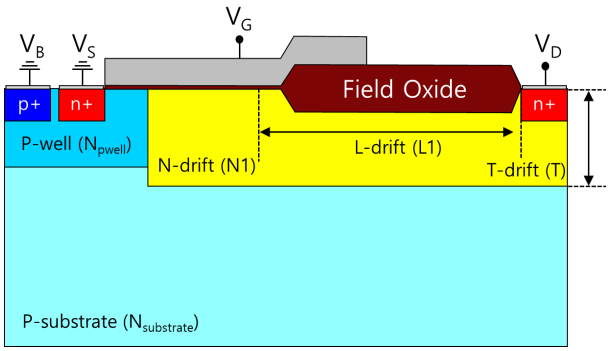

Fig. 1. Cross-sectional schematic of LDMOS device structure.

However, the performance of LDMOS is complexly determined by multiple process and structural parameters such as drift region length (L_{drift}), doping concentration (N_{drift}), gate length (L_g), P-well and substrate concentration (N_{PWELL}, N_{SUB}). Since these variables cause trade-offs among static and dynamic power characteristics such as breakdown voltage (BV), specific on-resistance (R_{on}), and gate-drain charge (Q_{gd}), it is difficult to find optimal design points that balance overall performance improvement using only conventional single-objective optimization or empirical design approaches [4], [5], [6].

Therefore, this study proposes an LDMOS device performance prediction and design framework that combines deep

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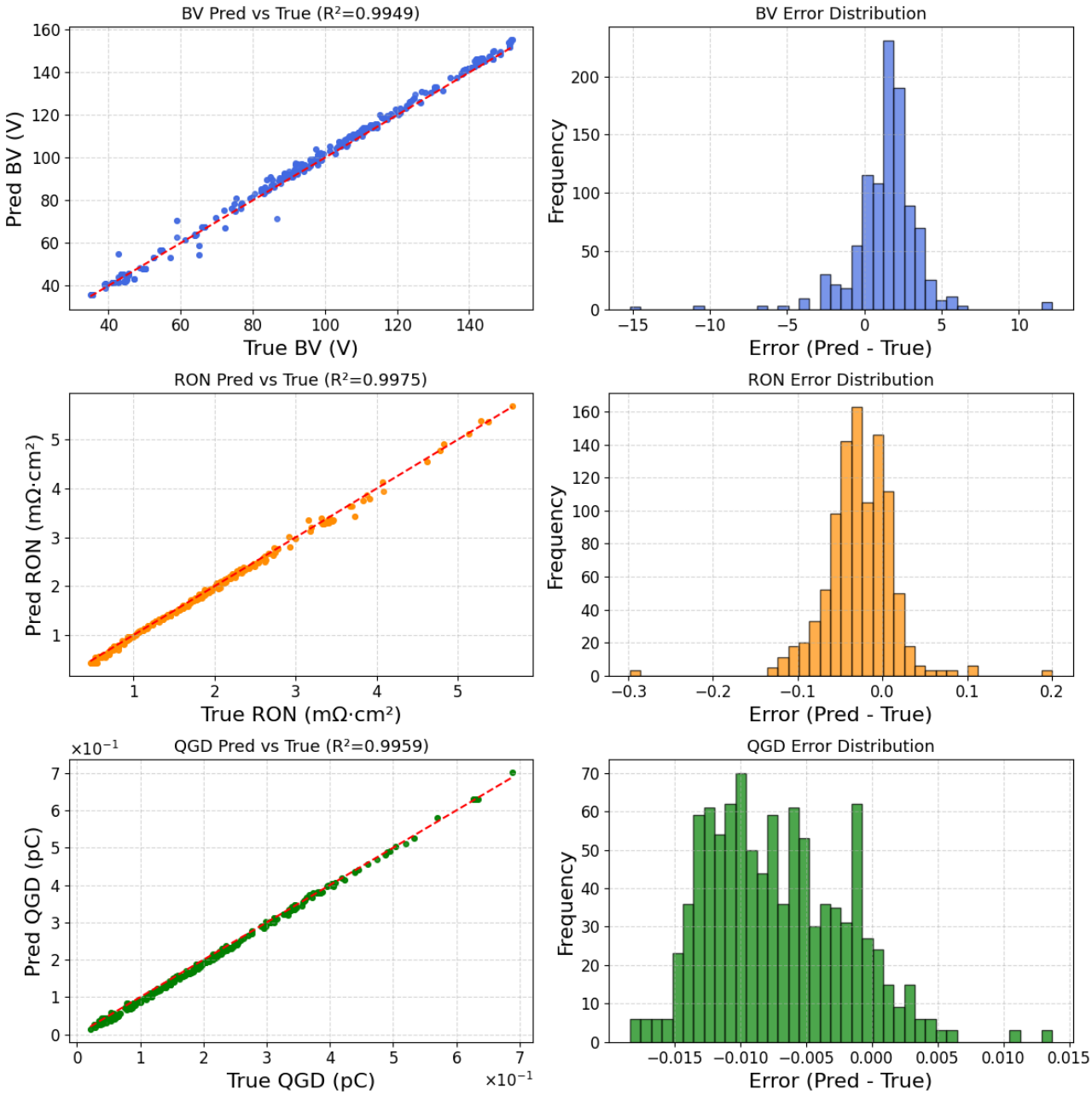

Fig. 2. Prediction accuracy of the ResNet-1D surrogate model. Left column: scatter plots comparing predicted versus true values for BV (top), RON (middle), and QGD (bottom). Right column: corresponding error distributions (Pred−True) for BV (top), RON (middle), and QGD (bottom). The model achieves $R^2 > 0.99$ for all outputs on the held-out test set.

learning-based surrogate models with multi-objective Pareto optimization techniques [7]. The deep learning-based surrogate model learns TCAD simulation data to approximate the non-linear correlations between design parameters and electrical characteristics with high precision, and enables model-based optimization by significantly reducing the parameter search space. Subsequently, by applying Pareto optimization techniques, the trade-off between static characteristics (BFOM = $\mathrm{BV}^2/R_{\mathrm{on}}$) and dynamic characteristics (SFOM = $Q_{\mathrm{gd}} \times R_{\mathrm{on}}$) is quantitatively analyzed, and a goal-aware design framework that can derive balanced optimal design points according to each application purpose is implemented [8], [9].

II. Device Structure and Simulation Method

The cross-sectional schematic of the simulated field-plate LDMOS device is shown in Figure 1. The device consists of highly doped n^+ source and drain regions, a lightly doped n-type drift region, a p-well region beneath the gate, and a p-type substrate.

To capture the complex trade-off relationships between structural configuration and electrical performance, five primary structural parameters were defined as input variables for device simulation and subsequent surrogate modeling: (1) drift length (L_{drift}, L1), the lateral extent of the drift region that primarily determines the breakdown voltage and on-resistance trade-off; (2) drift thickness (t_{drift}, T), the vertical dimension of the drift region that affects current spreading and resistance; (3) drift concentration (N_{drift}, N1), the doping concentration in the drift region that influences both depletion width and conductivity modulation; (4) p-well concentration (N_{pwell}, NPWELL), the doping level in the p-well region beneath the gate that impacts threshold voltage and channel characteristics; and (5) substrate concentration ($N_{\text{substrate}}$, NSUB), the background doping of the p-type substrate that affects punch-through behavior and backside electric field distribution.

The output parameters selected for model training and performance evaluation are breakdown voltage (BV), specific on-resistance (R_{on}), and gate–drain charge (Q_{gd}). These three output variables comprehensively represent the device trade-off between static power performance (characterized by BV and R_{on}) and dynamic switching behavior (represented by Q_{gd}).

A TCAD dataset of 1,000 samples is generated by random sampling of the five input parameters (L1, N1, T, NPWELL, and NSUB) within the following ranges: L1 = 8.0–16.0 μm, N1 = 7.5×10^{15}–5.0×10^{16} cm^{-3}, T = 1.5–3.5 μm, NPWELL = 1.5×10^{17}–6.5×10^{17} cm^{-3}, and NSUB = 3.0×10^{15}–3.0×10^{16} cm^{-3}. TCAD runs that did not converge or produced non-physical outputs were discarded to ensure dataset quality. The dataset is split into training/test = 80/20, and all preprocessing (e.g., normalization/standardization) is fitted on the training set only to avoid data leakage. Unless otherwise stated, all predictive results in Section III are reported on the held-out test set. In addition, all Pareto-optimal designs reported in this work are confirmed to lie within the min–max bounds of the training data for each input parameter (i.e., within the interpolation regime of the surrogate model).

Device simulations were performed using Synopsys Sentaurus TCAD with a 2D structure. To comprehensively account for carrier transport, high-field effects, and breakdown mechanisms in the field-plate LDMOS device, the following eight physics models were activated: (1) high-field saturation, (2) vertical electric field dependence (Enormal model), (3) effective intrinsic density (Oldslotboom model), (4) velocity saturation, (5) drift–diffusion transport model, (6) Shockley–Read–Hall (SRH) recombination, (7) Auger recombination, and (8) avalanche generation (impact ionization).

III. Results and Discussion

A. DNN-based surrogate model construction

The surrogate model was constructed to take five structural parameters (L_1, N_1, T, N_{PWELL}, N_{SUB}) as inputs and predict three key electrical characteristics—breakdown voltage (BV), gate–drain charge (Q_{GD}), and on-resistance (R_{ON})—as outputs.

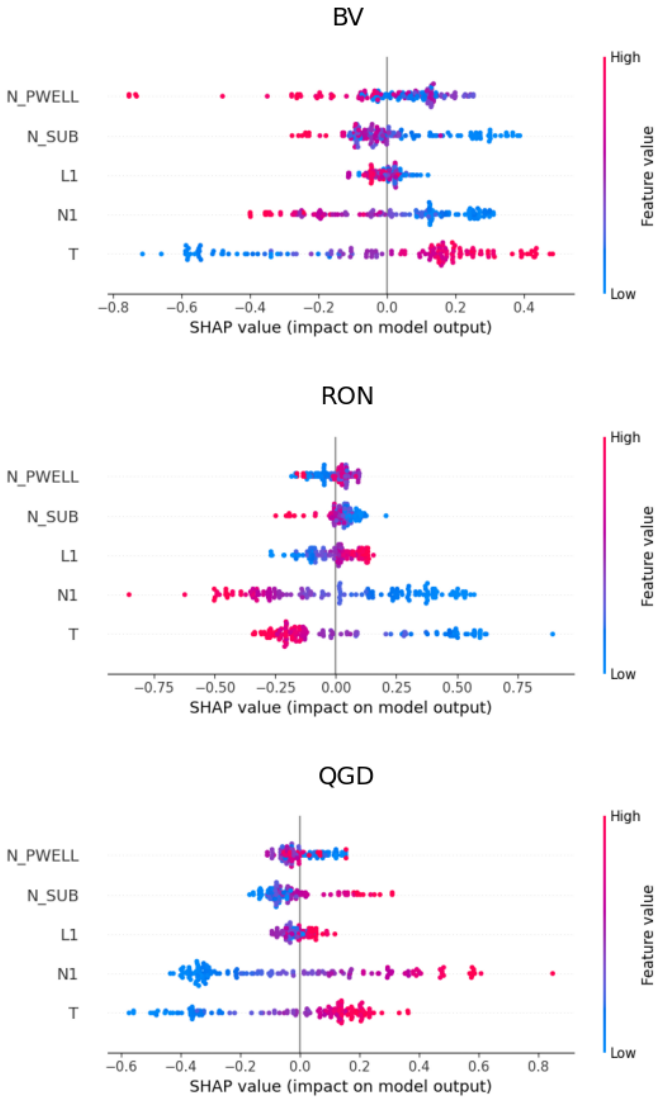

Fig. 3. SHAP analysis results revealing the relative importance of five input parameters on (top) breakdown voltage (BV), (middle) on-resistance (R_{ON}), and (bottom) gate-drain charge (Q_{GD}). The drift thickness T dominates BV prediction, while channel doping N_1 primarily controls R_{ON} and Q_{GD}.

The proposed model employed a 1D convolution-based ResNet (Residual Network) architecture, consisting of four stages of residual blocks expanding through 64–128–256–512 channels after the input layer, followed by fully connected layers. Each block includes two convolutional layers (Conv1d, kernel=3), batch normalization (BatchNorm1d), and ReLU activation functions, and is designed to prevent gradient vanishing in deep networks through skip connections.

To quantify the computational benefit of the proposed surrogate model, we measured the average wall-clock time per design for (i) TCAD simulation and (ii) ResNet-1D inference under the same workstation environment. The TCAD time denotes the end-to-end runtime (including simulation and post-

TABLE I
MEASURED RUNTIME PER DESIGN POINT FOR TCAD SIMULATION AND SURROGATE INFERENCE (BV, RON, AND QGD).

Metric	TCAD time	ResNet-1D time	Speedup
BV	31 min (1860 s)	45 s	41.3×
RON	13 min (780 s)	36 s	21.7×
QGD	48 min (2880 s)	54 s	53.3×

TABLE II
PREDICTION PERFORMANCE OF THE PROPOSED RESNET-1D SURROGATE MODEL ON THE HELD-OUT TEST SET.

Metric	R^2	NRMSE (range) [%]	MAPE [%]
BV	0.9949	2.99	2.39
RON	0.9975	1.25	4.81
QGD	0.9959	3.34	2.42

processing) required to obtain each target metric (BV, R_{ON}, and QGD) for a single design point. The ResNet-1D time denotes the end-to-end inference time to predict the same metric for the same one-design unit. The measured runtimes and speedups are summarized in Table I.

As shown in Fig. 2, the proposed ResNet-1D surrogate model achieved high prediction accuracy for all output variables. On the held-out test set, the coefficient of determination (R^2) exceeded 0.99 for BV, R_{ON}, and Q_{GD}, and the predicted values closely matched the TCAD simulation results. The mean absolute percentage error (MAPE) was 2.39% for BV, 4.81% for R_{ON}, and 2.42% for Q_{GD} (Table II). Overall, these results indicate that the proposed DNN-based surrogate model effectively learned the nonlinear interactions between design parameters, validating it as a reliable predictive model capable of replacing costly TCAD simulations. The prediction performance on the held-out test set is summarized in Table II.

B. Pareto-front exploration

To interpret the internal prediction characteristics of the surrogate model, SHAP (SHapley Additive exPlanations) analysis was performed. By quantifying the relative influence of the five input variables on each output value (BV, Q_{GD}, R_{ON}), the drift thickness T was identified as the most influential factor affecting BV. This is because the RESURF (Reduced Surface Field) condition significantly changes with variations in drift region thickness, making the electric field distribution and breakdown voltage characteristics most sensitive to this parameter.

Meanwhile, both R_{ON} and Q_{GD} responded most sensitively to N_1 (doping concentration near the channel). This is because N_1 directly affects channel resistance and gate–drain charge, thereby jointly determining switching speed and conduction loss characteristics. Therefore, it was confirmed that BV is primarily controlled by the structural factor T, while R_{ON} and Q_{GD} are mainly controlled by the electrical factor N_1. These results are summarized in Fig. 3.

Additionally, Fig. 4 presents the Pareto optimization results between BFOM (maximization) and SFOM (minimization). All candidate designs evaluated by the surrogate model during SMPSO are plotted as gray points. From this set, Pareto-optimal (non-dominated) solutions are extracted using the dominance criterion: a solution is non-dominated if there exists no other candidate with BFOM $\geq$ and SFOM $\leq$ simultaneously (with at least one strict inequality). The blue and red markers correspond to the two extreme Pareto solutions, i.e., the maximum-BFOM and minimum-SFOM points, respectively. The resulting front confirms the inherent trade-off: improving conduction efficiency via higher BV and lower R_{ON} tends to increase switching loss (captured by SFOM), whereas reducing switching loss generally degrades conduction efficiency. Therefore, selecting an appropriate operating point on the Pareto front is essential for balancing high-voltage tolerance and high-speed switching in LDMOS design.

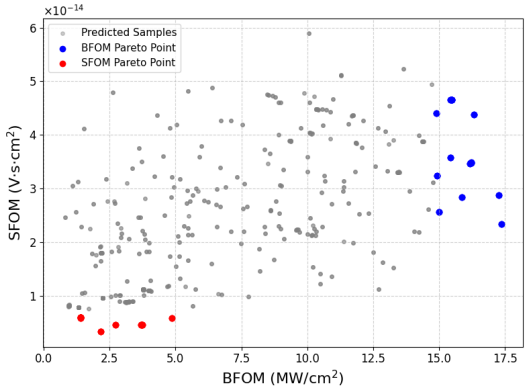

Fig. 4. Pareto optimization results between BFOM (to be maximized) and SFOM (to be minimized). Gray points denote all surrogate-evaluated candidate designs generated during SMPSO. Pareto-optimal (non-dominated) solutions are defined as designs for which no other candidate achieves a higher BFOM while simultaneously achieving a lower SFOM (with at least one strict improvement). The **blue** marker highlights the Pareto solution with the maximum BFOM, and the **red** marker highlights the Pareto solution with the minimum SFOM, illustrating the trade-off between conduction efficiency and switching loss.

IV. CONCLUSION

In this study, a deep learning-based surrogate model was developed to efficiently predict the electrical characteristics of LDMOS devices as a function of key process and structural parameters, and a multi-objective optimization analysis was performed using this model. The proposed ResNet-1D surrogate simultaneously predicts three outputs—breakdown voltage (BV), gate–drain charge (Q_{GD}), and on-resistance (R_{ON})—from five input variables (L_1, N_1, T, N_{PWELL}, N_{SUB}). The results on the held-out test set demonstrated that the coefficient of determination (R^2) exceeded 0.99 for all outputs, confirming that the surrogate model accurately approximates TCAD simulation results.

Through SHAP analysis, the internal decision-making structure of the model was quantitatively interpreted. The results showed that BV responds most sensitively to changes in drift thickness T, which is attributed to the significant variation in RESURF effect and electric field distribution according to drift region thickness. In contrast, R_{ON} and Q_{GD} were

most strongly influenced by the doping concentration near the channel N_1, indicating that this parameter acts as a key factor jointly determining channel resistance and switching speed.

Furthermore, based on the prediction results, BFOM and SFOM were defined and Pareto optimal analysis was performed. The analysis revealed that the two metrics exhibit a trade-off relationship, where increasing conduction efficiency (BFOM) increases switching loss (SFOM), and conversely, reducing SFOM decreases BFOM. This confirms that determining the balance point between high-voltage tolerance and high-speed switching characteristics is the key to LDMOS structure optimization.

Consequently, the proposed DNN-based surrogate model achieved a measured computational speedup of **21.7×–53.3×** over TCAD simulation while maintaining high prediction accuracy (Table I). The framework also provides an integrated analysis pipeline that interprets the physical influence of design-parameter variations and enables exploration of multi-objective optimal designs. In future work, the model will be extended to reliability prediction under environmental factors such as process variations and thermal stress, and to dynamic Pareto optimization.

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