Design of a 3.5kW Low-Noise Current-Fed Converter for High-Integrity Data in AI-Based SOFC Systems

Geon Kim[1], Ryun Kang[1], Dongyeong Kim[1], Suyeon Kim[1], Jewon Park[1], Shinwook Kim[1], Sowon Kim[1], Chaehyuk Lim[1], Hyeona Seo[1], Jeonghyeon Yun[1], Juwon Lee[1], Hyerin Lee[1], Ujin Choi[2], Eojin Kim[2], Minwoo Jeong[2], and Myoungjin Lee[2,*]

[1]Dept. of Intelligent Electronics and Computer Engineering, Chonnam National University, Gwangju, South Korea
[2]Dept. of Electronics and Computer Engineering, Chonnam National University, Gwangju, South Korea

rjsdlchd@gmail.com, kang0228youn@jnu.ac.kr, gnodyoung@jnu.ac.kr, bollic4504@gmail.com, parkje0922@jnu.ac.kr, sinw1559@gmail.com, kjw333349049@gmail.com, lch9909@jnu.ac.kr, engine5kor@gmail.com, yunjunghyun0623@gmail.com, dlwndnjs2055@gmail.com, lhy2rin@gmail.com, ujinsuin@gmail.com, djwls1001@naver.com, blueminw07@naver.com, mjlee@jnu.ac.kr
*Corresponding author

***Abstract*—Solid Oxide Fuel Cells (SOFCs) are gaining significant attention as a key component of future generation systems due to their high efficiency and stable power delivery. However, their low-voltage, high-current output characteristics, coupled with the stringent requirement for minimal input current ripple to ensure cell lifespan, impose major constraints on the design of grid-tied power conversion systems (PCS), which are increasingly managed by AI algorithms for optimal load dispatch and system stability. Although a 1.5 kW Current-Fed Push-Pull (CFPP) converter previously achieved low ripple and high efficiency (96.5%), research on its scalability for high-power grid applications has been insufficient. This paper presents a parameter design methodology for scaling the 1.5 kW converter to a 3.5 kW class. The proposed design reflects recent industrial trends in SOFC stacks by elevating the input voltage from 54 V to 128 V, thereby reducing the system's conduction losses. The parameter design for magnetic, active, and passive components is detailed. The validity of the proposed design was verified through PSIM simulations and a 3.5 kW hardware prototype. Experimental results demonstrate that the proposed converter achieves a high efficiency of 96.7% at rated load. Furthermore, it was verified that the input current ripple—a critical requirement—was suppressed to an exceptionally low 2.4% of the nominal current. This confirms that the proposed design methodology can simultaneously satisfy the demands for high-power scalability and the strict ripple requirements of SOFCs, providing a robust hardware platform necessary for the implementation of advanced AI-based energy management.**

Keywords—Solid Oxide Fuel Cell (SOFC), Current-Fed Push-Pull Converter (CFPP), High Step-Up, Input Current Ripple, Parameter Design, Scalability, Saturation Cycling

I. INTRODUCTION

Driven by global carbon neutrality goals, the adoption of renewable energy sources to replace fossil fuels has accelerated. However, their inherent intermittency limits their viability as a stable baseload power source. In contrast, Solid Oxide Fuel Cells (SOFCs) are attracting significant attention as a key pillar of future generation systems, capable of providing stable power with high efficiency and density. However, the low-voltage, high-current DC output characteristic of SOFCs necessitates a power conversion system (PCS) for grid integration[1-2]. Furthermore, these power conversion systems face a stringent requirement to minimize the input current ripple, which is essential for preserving the fuel cell's lifespan and maintaining operational efficiency.

Beyond protecting the SOFC, this low input current ripple is critical for establishing a low-noise power foundation. High ripple inherently generates significant electromagnetic interference (EMI), which can corrupt the sensitive analog sensor data (e.g., current, voltage, temperature) used by system controllers. In AI-driven power systems, which serve as the critical interface to energy management systems (EMS), this data integrity is paramount. Flawed sensor data—caused by EMI—leads directly to erroneous AI-based diagnostics, flawed predictive control, and potential system instability. Therefore, designing a low-noise converter is a fundamental prerequisite for guaranteeing signal fidelity, which is essential for the successful deployment of intelligent management in modern power generation systems.

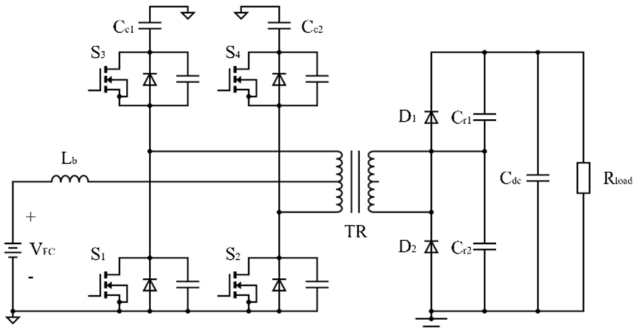


Fig. 1. The 3.5kW high-voltage current-type push-pull converter topology

In response to these industrial demands, a 1.5 kW current-fed push-pull DC/DC converter employing an active clamp circuit was developed[2]. This topology successfully achieved both high efficiency (96.5%) and minimized input current ripple. Furthermore, it was quantitatively verified that during the inevitable 'saturation cycling' phenomenon, the desired "zero" input current ripple and peak efficiency cannot be simultaneously achieved in the fuel cell system. However, the scalability of this topology for high-power applications has not yet been thoroughly discussed. As scalability is an indispensable factor for large-scale grid integration, this paper aims to present a design methodology to address this[3]. This work contributes to establishing scalability for practical industrial applications, moving beyond a simple performance verification of the previously developed converter.

II. PARAMETER DESIGN FOR 3.5KW-CLASS SCALING

The 3.5 kW converter proposed in this study reflects the recent industrial trend of elevating the stack's nominal output voltage—increasing from 54 V to 128 V—by expanding the number of series-connected unit cells. By raising the input voltage, the overall system current for the scaled-up power rating is reduced by more than 57%, which consequently mitigates the I^2R conduction losses. Furthermore, the output voltage has been increased to 700 V, determined by the modulation index requirements of the grid-tied inverter[4].

A. Magnetic Components

1) Boost Inductor (L_b): The core size of the boost inductor is determined by the energy it must store. Equation (1) represents the Area Product (A_p), which balances the magnetic cross-sectional area required to prevent saturation against the window area needed for the winding: [5]

$$A_{p\_Lb} = \left(\frac{L_b \cdot I_{Lb}^2}{B_{max} \cdot J \cdot K_u}\right)^{\frac{1}{x}} \quad (1)$$

By satisfying this criterion, the inductor can handle the peak current without magnetic saturation while minimizing volume. Based on this, the required core area product (A_p) for the boost inductor, A_{p_Lb}, when scaled up to 3.5 kW is $0.64\times 10^9 mm^4$. This confirms that the previously used core is sufficient for the new design. This offers a significant advantage in reducing the overall system volume and cost.

$$N_{b\_Lb} = \sqrt{\frac{L_b}{A_L}},\ B_{pk\_Lb} = \frac{L_b \cdot I_{pk}}{N_b \cdot A_c} < B_{sat} \quad (2)$$

The minimum required number of turns is calculated using the A_L-value of the existing core, and it is verified that saturation is avoided even under peak current conditions. Although the output power has increased, a sufficient saturation margin is secured, as the RMS input current does not significantly differ from that of the previous design.

2) Transformer : The transformer core size (Area Product, A_p) is determined by the switching frequency f_{sw} and the apparent power to be handled P_t.

$$A_{p\_TR} = \left(\frac{P_t \cdot 10^4}{K_f \cdot K_u \cdot B_{max} \cdot f_{sw} \cdot J}\right)^{\frac{1}{y}} \quad (3)$$

Based on this calculation, the required transformer core area product (A_{p_TR}) is 1.62×10^{10}mm^4, which necessitates a replacement of the existing core. Therefore, a PQ6273 core was selected in this paper.

$$I_{p\_rms} \approx \frac{I_{rms}}{2} \cdot \sqrt{2 \cdot D} \quad (4)$$

The minimum required number of turns must be determined by considering the increase in AC resistance due to the skin and proximity effects. To mitigate this issue, along with the challenges posed by high-frequency components on the secondary side, it is advantageous to utilize Litz wire or multiple parallel-connected windings. In this paper, two transformers are operated in parallel, and Litz wire is employed to alleviate the current stress on the windings.

TABLE I. PARAMETER DESIGN OF MAGNETIC COMPONENTS

Parameters of components	***Symbols***	***1.5kW class (reference)***	***3.5kW class (paper)***
Boost inductor core type	-	OR571F090	
Boost inductor saturation flux density [T]	B_{sat_bi}	1.5	
Boost inductor core volume [cm^3]	V_{core_bi}	28.6	
Boost inductor A_L-value [nH/N^2]	A_L	207	
Number of turns in the boost inductor	N_{b_Lb}	23	
TR core material	-	PQ - 3C95	PQ-6273
TR core volume [cm^3]	V_{core_TR}	37.1	106
TR turn ratio	n	2.6	1.5

B. Active Components

1) *MOSFETs:* The main switches (S_1, S_2) are responsible for the primary power transfer, while the auxiliary switches (S_3, S_4) handle leakage energy recovery and voltage clamping. These switches, connected in their respective legs, are subjected to the same voltage stress, which is expressed as follows[5]:

$$V_{DS} = V_{Cc} \approx \frac{V_{FC}}{1-D} \quad (5)$$

To accommodate the voltage stress, including potential overshoot, a safety margin of at least 1.5 times is applied. This necessitates selecting (or replacing the existing) MOSFETs with a V_{DS} breakdown voltage rating of at least 400 V.

$$I_{D\_rms} \approx I_{Lb\_rms} \times \sqrt{D},\ I_{D\_peak} \approx I_{Lb\_rms} \times 1.3, \quad (6)$$

Regarding the current stress, the device (MOSFET) is selected based on its drain current (I_D) rating, which must satisfy two conditions simultaneously: 1) a margin of at least three times the RMS current, and 2) the peak current, assuming a specific ripple (e.g., 30% in this paper). Furthermore, to minimize conduction losses, a device with the lowest possible $R_{DS(on)}$ (on-state resistance) must be chosen.

2) Diodes : In the voltage doubler topology, when one diode is conducting, the other diode must block the entire output voltage. Therefore, to ensure reliability, a safety margin of at least 1.5 times is applied, which mandates the selection of diodes with a breakdown voltage rating of at least 1050 V. Although the output current is relatively low due to the high-voltage nature of the converter, a device with a low forward voltage (V_f) is selected to minimize conduction losses. Furthermore, since Zero-Current Switching (ZCS) is achieved on the secondary side, the reverse recovery losses are negligible. Consequently, the reverse recovery time (t_{rr}) is not a critical selection criterion. Considering these factors, the previously utilized diodes already satisfy all the aforementioned requirements and are therefore sufficient for this design.

TABLE II. PARAMETER DESIGN OF ACTIVE COMPONENTS

Parameters of components	***Symbols***	***1.5kW class (reference)***	***3.5kW class (paper)***
MOSFET breakdown voltage [V]	V_{DS}	150	650
MOSFET continuous drain current [A]	I_d	171	75
MOSFET on-resistance [mΩ]	$R_{ds(on)}$	4.8	17
MOSFET gate charge [nC]	Q_g	151	215
Diode repetitive peak reverse voltage [V]	V_r	1200	
Diode average forward current [A]	I_o	62	
Diode forward voltage [V]	V_f	1.65	

C. Passive Components

1) Clamp Capacitor C_c : The clamp capacitor, connected to the auxiliary switch, absorbs the energy stored in the transformer's primary-side leakage inductance (L_{lk}). This action alleviates the voltage stress across the main switches. The energy stored in the leakage inductance, which causes voltage spikes across the main switches during turn-off, is expressed as follows [6]:

$$E_{lk\_Cc} = \frac{1}{2} L_{lk\_pri} \cdot I^2_{peak\_pri} \quad (7)$$

To effectively absorb this energy and clamp the voltage spike within the safety margin defined in Eq. (5), the capacitor size

must be proportional to this leakage energy. Assuming the leakage inductance (L_{lk_pri}) is doubled—a consequence of the larger physical size required for the increased output power—the energy storage requirement increases by more than twofold. Consequently, the capacitance of the clamp capacitor (C_c) must also be doubled. Furthermore, as the input voltage level has approximately doubled, the capacitor's DC voltage rating must also be increased by a factor of at least two.

2) Resonant Capacitor C_r : As the transformer turns ratio is reduced, the leakage inductance reflected to the secondary side also decreases. The design of C_r follows the methodology proposed in the reference study, which is expressed as follows:

$$C_{r1} = C_{r2} = \frac{\left(\frac{D}{f_{sw}} - t_D\right)^2}{2\pi^2 L_{lk}} \tag{8}$$

Consequently, the secondary-side diodes achieve Zero-Current Switching (ZCS) across the entire load range. This effectively eliminates the losses caused by reverse recovery current.

TABLE III. PARAMETER DESIGN OF PASSIVE COMPONENTS

Parameters of components	***Symbols***	***1.5kW class (reference)***	***3.5kW class (paper)***
Clamp capacitor capacitance [μF]	C_C	20	40
Clamp capacitor voltage rating DC [V]	V_{Cc}	250	500
Clamp capacitor ESR [mΩ]	R_{Cc_ESR}	2.4	2
Resonance capacitor capacitance [μF]	C_r	3.1	4
Resonance capacitor voltage rating DC [V]	V_{Cr}	1000	500

III. SIMULATION AND EXPERIMENTAL VERIFICATION

To validate the feasibility of the parameter design derived in Section II and to analyze the transient response before hardware implementation, a simulation model was constructed. The simulation was verified using PSIM 9.1.1 and was conducted based on the parameters and components specified in Section II: P_o = 3.5 kW, V_{in} = 128 V, and V_o = 700 V. The experimental prototype was designed with the same specifications. To validate the operational margin, the hardware was tested under conditions ranging from no-load up to a 105% overload.

A. Simulation results

The simulation results are plotted in a single graph, as shown in Fig. 2, to facilitate a comparison between the conventional converter and the newly designed high-power converter. In this figure, the data pertaining to the conventional converter is represented by blue-toned traces, while the data for the converter proposed in this paper is shown in red-toned traces.

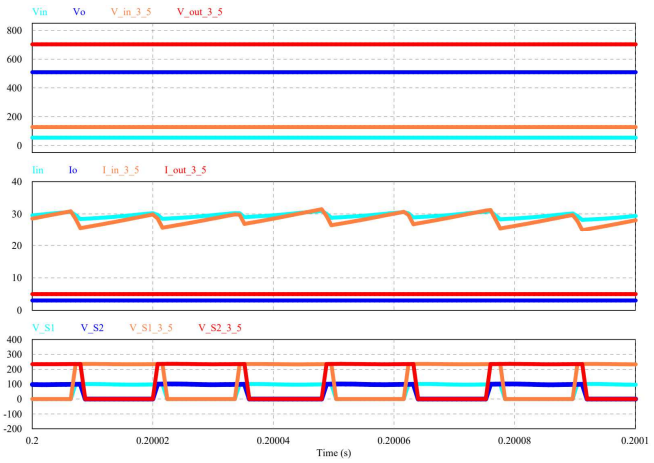


Fig. 2. 3.5kW high-voltage current-type push-pull converter simulation waveforms: input/output voltage, input/output current, main switch S_1, S_2 V_{DS} waveforms

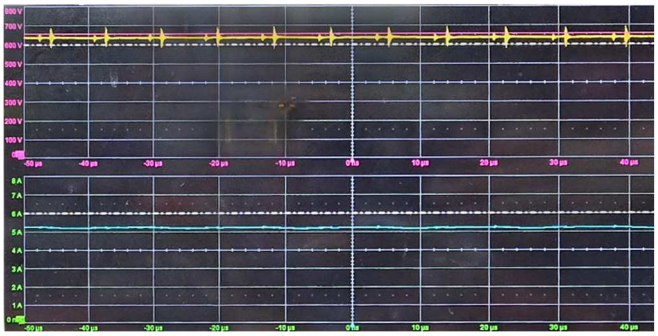
Typically, the transformer turns ratio (n) is determined based on the duty cycle (D) corresponding to the peak efficiency point at rated output power. Through this, it was confirmed that the converter successfully provided the intended output voltage relative to the input. Additionally, it was verified that the voltage stress on the main switches scaled in accordance with the higher input voltage level. The input current ripple measured in the simulation was approximately 14% of the nominal current. This simulated value is considered conservative, as it is common for the unmodeled parasitic inductances of the physical hardware to provide additional damping, resulting in a lower ripple in practice.

B. Experimental results

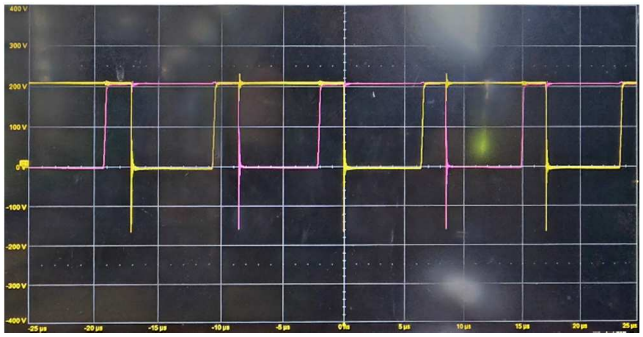
To experimentally validate the design and simulation results, the input and output voltage and current waveforms, as well as the drain-source voltage (V_{DS}) waveforms of the main switches (S_1, S_2), were measured. These measurements were captured using an HDO4104A oscilloscope, a CP150 current probe, and an HVD3106A high-voltage differential probe.

Fig. 3(a) presents the measured waveforms. Specifically, as shown in the detailed switching waveforms of Fig. 3(b), the input voltage (V_{in}) exhibits ringing of approximately 18% during transients. However, the output voltage (V_{out}, Red trace), which serves as the power bus for the AI system, remains tightly regulated and stable. This confirms that the converter effectively isolates the load from input-side transients.

Furthermore, for the fuel cell side, the input current (I_{in}, Blue trace) ripple—the critical factor for stack longevity—is suppressed to an exceptionally low 2.4%. Regarding the potential for EMI affecting the control system, the sensing architecture utilizes galvanically isolated interfaces (e.g., Hall sensors). This structure effectively decouples the control ground from the power stage, ensuring that the high-frequency switching noise at the input does not corrupt the sensor data fed into the AI algorithms.



(a)



(b)

Fig. 3. Experimental waveforms. (a) Steady-state operation showing input/output voltage and current. (b) Detailed switching transients. Key traces: Input Voltage (V_{in}, Yellow), Output Voltage (V_{out}, Red), Input Current (I_{in}, Blue), and Output Current (I_{out}, Green). Note the stable output voltage (V_{out}) despite the input ringing.

Fig. 4. Efficiency of a 3.5kW high-voltage current-type push-pull converter measured using a power analyzer

Furthermore, the efficiency at full load was measured using a WT1804E power analyzer. The converter proposed in this paper, scaled to 3.5 kW, achieved an efficiency of 96.7%, whereas the reference study exhibited 96.5% efficiency. This signifies that the objectives of this paper—achieving output power scalability and improved efficiency while maintaining minimal input current ripple—have both been successfully attained.

IV. CONCLUSION

This paper presented and experimentally validated a parameter design methodology for scaling a high step-up current-fed push-pull converter to a 3.5 kW class for SOFC grid-tied systems. To overcome the limitations of the previous 1.5 kW converter (54 V input), a strategy was employed to elevate the input voltage to 128 V, thereby reducing the system's I^2R conduction losses. Accordingly, the process of redesigning the parameters for key components—including the boost inductor, transformer, MOSFETs, and capacitors—to fit the scaled-up power level was detailed. A 3.5 kW prototype was fabricated to validate the design, and tests were conducted under rated load and 105% overload conditions. The experimental results confirmed that the proposed 3.5 kW converter achieved a peak efficiency of 96.7%, demonstrating an improvement over the 1.5 kW type (96.5%). Furthermore, the input current ripple, which is critical for SOFC longevity, was verified to be suppressed to an exceptionally low 2.4% of the nominal current.

TABLE IV. PERFORMANCE COMPARISON TABLE

Parameter	***Previous Converter [2]***	***Proposed Design***
Power Rating [kW]	1.5	3.5
Input Voltage [V]	54	128
Input Current Ripple (target) [%]	4.6	2.4
Efficiency (Peak) [%]	96.5	96.7

This low-noise characteristic is a key enabler for robust AI integration. By minimizing conducted EMI at the source, the proposed converter ensures the high signal integrity required for the sensors and communication networks that feed data to AI management systems, thereby validating its role as a reliable hardware platform for intelligent power control. This demonstrates that the proposed design methodology successfully satisfies the dual requirements of high-power scalability and low input current ripple. Although switching transients were observed on the input voltage, the experimental results confirmed that both the output voltage stability for the AI load and the input current quality for the SOFC were successfully maintained. Future work will further enhance the system by suppressing EMI generation at the source. This includes optimizing the PCB layout to minimize stray inductance and implementing active gate driving techniques to actively dampen transients. These measures will maximize the signal-to-noise ratio (SNR), ensuring robust communication for distributed AI control networks.

Optimizing the snubber circuit, gate driver, and PCB layout to mitigate this ringing across all load conditions is a complex multi-objective problem. Therefore, future work will focus not only on passive component optimization but also on the development of an AI-based adaptive control strategy. This controller, potentially using reinforcement learning or a neural network model trained on the hardware's operational data, will aim to actively dampen these transients in real-time. This intelligent control approach is expected to significantly enhance system stability and efficiency beyond what is achievable with static hardware tuning, enabling the converter to fully support dynamic, AI-managed power systems.

ACKNOWLEDGMENT

This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education(RS-2025-25398164). This work was supported in part by the MSIT(Ministry of Science and ICT), Korea, under the ICAN(ICT Challenge and Advanced Network of HRD) support program(IITP-2025-RS-2022-00156385) supervised by the IITP(Institute for Information & Communications Technology Planning & Evaluation) This research was supported by the Ministry of Science and ICT (MSIT), Korea, under the Innovative Human Resource Development for Local Intellectualization support program (IITP-2025-RS-2022-00156287) supervised by the Institute for Information &

communications Technology Planning & Evaluation (IITP) This research was supported by Korea Institute for Advancement of Technology(KIAT) grant funded by the Korea Government(Ministry of Education) (P0025690, Semiconductor-Specialized University)

REFERENCES

[1] R.-J. Wai, C.-Y. Lin and C.-C. Chu, "High step-up DC-DC converter for fuel cell generation system," *in Proc. of IEEE 30th Annual Conf. of Industrial Electronics Society (IECON)*, vol. 1, pp. 57–62, Busan, South Korea, November 2004.

[2] G. Kim, D. J. Kim, R. Y. Kim, and M. J. Lee, "Impact of duty ratio and saturation cycling on efficiency in current-fed push-pull DC/DC converter with active-clamp," *IEEE Transactions on Power Electronics*, 2025.

[3] Q. Wu, Q. Wang, J. Xu, H. Li and L. Xiao, "A high-efficiency step-up current-fed push–pull quasi-resonant converter with fewer components for fuel cell application," *IEEE Trans. on Industrial Electronics*, vol. 64, no. 8, pp. 6639–6648, August 2016.

[4] C.-T. Pan, C.-F. Chuang and C.-C. Chu, "A novel transformer-less adaptable voltage quadrupler DC converter with low switch voltage stress," *IEEE Trans. on Power Electronics*, vol. 29, no. 9, pp. 4787–4796, September 2013.

[5] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, December 2017.

[6] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. on Industrial Electronics*, vol. 61, no. 5, pp. 2307–2315, May 2013.