Analysis of Total Ionizing Dose Effects Based on the Thickness of the STI Region in Buried Channel Array Transistors

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***Abstract*—This study explores the impact of Shallow Trench Isolation (STI) thickness on Total Ionizing Dose (TID) effects in Buried Channel Array Transistor (BCAT) structures using TCAD simulations. The findings reveal that increasing STI thickness results in higher leakage currents due to enhanced charge trapping and a significant reduction in electron density, with electron density showing greater sensitivity to STI variations. A reduction in STI thickness from 500nm to 100nm improved leakage current by over 29% while reducing electron density by 99.7%, highlighting the critical role of STI optimization. Thicker STI layers, with their larger oxide volumes, are more prone to radiation-induced degradation, whereas thinner STI effectively mitigates TID effects and improves radiation tolerance. This study underscores the importance of STI thickness optimization in designing high-reliability, radiation-hardened semiconductors for extreme environments, such as space, while providing a foundation for advancing radiation-resistant semiconductor technologies.**

Keywords—Buried Channel Array Transistor, STI (Shallow Trench Isolation), Total Ionizing Dose (TID) Effects

I. INTRODUCTION

The rapid advancements in process technology have enabled the development of highly integrated memory semiconductors, such as DRAM, through progressively smaller process nodes [1]. These miniaturized technologies have become essential for achieving high performance and integration density, establishing a crucial trajectory for commercial semiconductor advancements. However, semiconductors designed for use in space environments must prioritize reliability and stability under extreme conditions, which often necessitates maintaining significantly larger process dimensions compared to their commercial counterparts. This disparity in process scales introduces critical differences in how these devices respond to radiation, particularly in the context of **Total Ionizing Dose (TID)** effects, which necessitates detailed analysis to ensure optimal performance and reliability [2], [3], [4], [5].

Radiation environments induce TID effects in semiconductor devices, resulting in the generation of electron-hole pairs within the oxide layers. These charges become trapped at the oxide/semiconductor interface and within the oxide itself, leading to degradation in the electrical characteristics of the device, including increased leakage current and reduced performance. The extent of these effects is influenced not only by process dimensions but also by the structural configuration of the device. In particular, the **Buried Channel Array Transistor (BCAT)** structure, characterized by its deep channel design and critical role in high-density devices, provides a valuable framework for studying these effects [6].

One of the key structural elements within BCAT devices is the **Shallow Trench Isolation (STI)**, an oxide insulator that occupies a significant volume of the device. The thickness of the STI layer directly impacts the radiation-induced charge trapping behavior, as a larger oxide volume allows for greater electron-hole pair generation and accumulation, exacerbating leakage current issues. Despite its critical role, the influence of STI thickness on TID-induced degradation remains underexplored, particularly within the BCAT structure, where understanding the interplay between geometry and radiation response is essential [7].

This study aims to systematically investigate the impact of STI thickness on the TID-induced performance degradation of BCAT structures. Using advanced TCAD simulations, we analyze how varying STI thickness influences charge trapping behavior, leakage currents, and overall device reliability under radiation exposure. By identifying the relationship between STI dimensions and radiation effects, this work provides valuable insights for optimizing device structures to enhance radiation tolerance. The findings of this study are expected to contribute to the development of high-reliability semiconductors capable of stable operation in extreme environments, such as space,

while laying the groundwork for future advancements in radiation-hardened semiconductor technologies.

II. Device Structures And Simulation Setup

A. Device Structure)

From the perspective of device structure, we adopted the parameters outlined in Table I [2], [8]. Additionally, to simulate the movement of charge carriers within the oxide, we performed TCAD simulations using OxideAsSemiconductor in place of the conventional oxide [1].

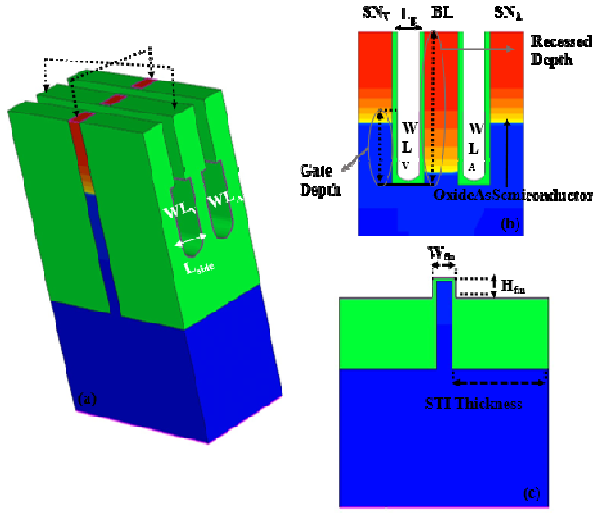

Fig. 1. (a) Three-dimensional (3D) structure of BCAT. (b) Cross-sectional view across the gate. (c) Cross-sectional view of the fin body.

Figure 1(a) presents a three-dimensional (3D) schematic of the BCAT structure. As shown in Figures 1(a) and 1(b), the aggressor word line (WL_A) refers to the cell that is repeatedly activated, while the victim word line (WL_V) is the cell affected by WL_A, leading to reliability issues [8]. In the Pi-BCAT device, the green-colored regions represent the gate oxide and the Shallow Trench Isolation (STI). Notably, the STI occupies the majority of the oxide region in the device.

B. Simulation Setup

Sentaurus TCAD was employed to simulate the BCAT structure, where the cell is designed with a saddle-fin (buried metal word line) configuration, sharing a common active area and bit line (BL). The devices analyzed in this study incorporate reliable source/drain (S/D) doping concentrations, modeled with Gaussian profiles to accurately replicate the typical I–V characteristics of DRAM [8].

Table I lists the device parameters and bias conditions for the RHE simulation that were previously used. In the TCAD device simulation, we integrated the following models: 1) bandgap narrowing (slot-boom); 2) Shockley–Read–Hall recombination (doping- and temperature-dependent field enhancement); 3) band-to-band tunneling (Hurkx); 4) doping-dependent mobility (Masetti) and mobility degradation; 5) velocity saturation; 6) drift-diffusion; 7) Auger recombination; 8) avalanche generation; and 9) Radiation. The TID effects was simulated using 3D TCAD mixed-mode simulations [8].

TABLE I
Device Parameters And Bias Conditions For Simulations [2]

Parameter	Value
Gate oxide thickness	4 nm
L_g	18 nm
L_{side}	34 nm
W_{fin}	18 nm
H_{fin}	18 nm
W_{side}	7nm
Recessed depth	150 nm
Gate depth	80 nm
Metal gate WF	4.6 eV
N-type Peak Doping Concentration	$1x10^{20}cm^{-3}$
P-type Peak Doping Concentration	$5x10^{17}cm^{-3}$
Temperature	300K
Radiation Type	Gamma-rays
STI Thickness	100nm~500nm

III. RESULTS AND DISCUSSION

A. Analysis of Simulation STI Thickness Change

The variation in leakage current of BCAT with respect to STI thickness under TID conditions was compared and analyzed.

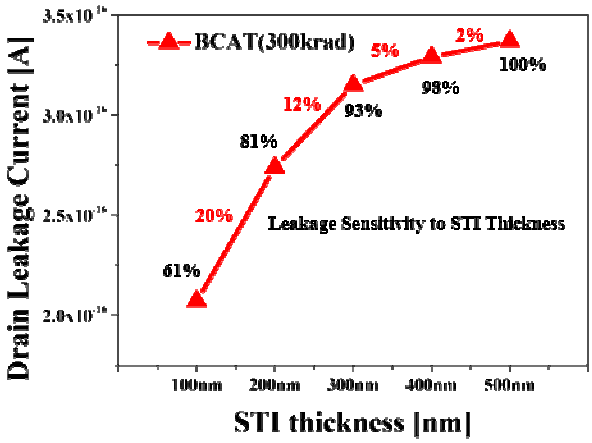

Fig. 2. TID-Induced Leakage Current Variation with STI Thickness in BCAT at BL = 0.6V, WL_A = -0.2V, and WL_V = -0.2V.

Figure 2 illustrates the variation in TID-induced leakage current with respect to STI thickness at a radiation dose of 300 krad, with WLA and WLV voltages set to -0.2V. In BCAT, the leakage current increases with STI thickness. Notably, the leakage current characteristics of BCAT show an improvement of over 29% when the STI thickness is reduced from 500nm to 100nm. This indicates that thicker STI structures are more susceptible to TID effects. Furthermore, as the STI thickness decreases, the leakage current exhibits a steeper decline, with the improvement rate increasing from an initial 5% to as much as 29%. This indicates that reducing the STI thickness can significantly enhance the leakage current characteristics of BCAT.

B. Carrier Distribution within Oxide

This variation can be explained by the increase in the oxide volume exposed to TID effects as the STI thickness increases. A larger oxide volume provides more space for radiation-induced charge carriers, resulting in a higher probability of electron-hole pair generation. These pairs, in turn, contribute to increased charge trapping at the oxide/semiconductor interface and within the oxide itself [3]. As trapped charges accumulate, they degrade the electrical properties of the device, such as leakage current. Therefore, a detailed analysis was conducted to quantify the amount of trapped electrons within the oxide and at the interface for varying STI thicknesses, providing further insight into the impact of STI thickness on TID-induced degradation.

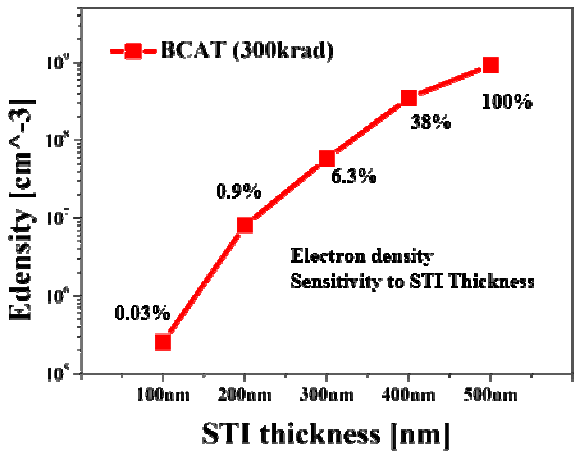

Fig. 3. TID-Induced Electron density Variation with STI Thickness in BCAT at BL = 0.6V, WL_A = -0.2V, and WL_V = -0.2V.

Figure 3 illustrates the variation in electron density caused by TID effects at a radiation dose of 300 krad, with WLA and WLV voltages set to -0.2V, as a function of STI thickness. As previously discussed, in BCAT, leakage current increases with STI thickness. This behavior can be attributed to a significant decrease in electron density, or carrier concentration, within the oxide as STI thickness increases. Specifically, while Figure 2 shows a 29% improvement in leakage current characteristics when the STI thickness is reduced from 500nm to 100nm, Figure 3 reveals a drastic 99.7% reduction in electron density over the same range. This stark difference indicates that electron density is significantly more sensitive to STI thickness variations compared to leakage current.

The sharp decline in electron density with decreasing STI thickness suggests that thicker STI structures exacerbate charge trapping and carrier recombination caused by TID effects. A larger oxide volume in thicker STI structures provides more sites for radiation-induced charge trapping, resulting in a substantial reduction in free carrier concentration. Consequently, this leads to higher leakage currents and greater performance degradation.

Furthermore, as STI thickness decreases, leakage current demonstrates a steeper decline, with the improvement rate increasing from an initial 5% to as much as 29%. This underscores the critical role of STI thickness optimization in enhancing the leakage current characteristics of BCAT devices. Simultaneously, the reduction in electron density highlights the necessity of understanding the interplay between charge trapping mechanisms and carrier dynamics to minimize TID-induced degradation. These results strongly indicate that minimizing STI thickness can significantly enhance the radiation tolerance of BCAT structures, providing a pathway for designing more reliable devices in extreme environments such as space.

C. Equations

The equations are an exception to the prescribed specifications of this template. You will need to determine whether or not your equation should be typed using either the Times New Roman or the Symbol font (please no other font). To create multileveled equations, it may be necessary to treat the equation as a graphic and insert it into the text after your paper is styled.

IV. CONCLUSION

This study systematically analyzed the impact of Shallow Trench Isolation (STI) thickness on Total Ionizing Dose (TID) effects in Buried Channel Array Transistor (BCAT) structures. Through TCAD simulations under radiation conditions, it was confirmed that increasing STI thickness results in higher leakage currents, primarily due to charge trapping and a significant reduction in electron density. Notably, when STI thickness was reduced from 500nm to 100nm, leakage current characteristics improved by over 29%, while electron density decreased by 99.7%, indicating a pronounced sensitivity of electron density to STI thickness variations.

Thicker STI structures provide a larger oxide volume, which increases the likelihood of radiation-induced electron-hole pair generation and trapping, thereby accelerating performance degradation in radiation environments. Conversely, reducing STI thickness can significantly enhance leakage current characteristics, highlighting the importance of STI thickness optimization in improving the radiation tolerance of BCAT structures.

These findings emphasize that optimizing STI thickness is a critical design parameter for enhancing the reliability of semiconductor devices in extreme environments. For applications such as space, where radiation reliability is paramount, this study provides valuable insights for designing efficient and reliable high-performance devices. Future research should explore additional structural and process parameters affecting trapping mechanisms and carrier dynamics to develop more comprehensive strategies for improving radiation tolerance.

This work offers foundational data for designing high-reliability semiconductors in extreme environments and is expected to contribute to advancements in radiation-hardened semiconductor technologies.

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