Image Synthesis with Single-type Patterns for Mixed-type Pattern Recognition on Wafer Bin Maps

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***Abstract*—To increase the productivity, it is important to manage yield and reduce defects in the semiconductor industry. One of the efforts is to identify defect patterns and control the cause factors that affects the defects. Many engineers inspect the quality of each chip and check the defect pattern on the wafer bin maps. To get the accurate and consistent classification results regardless of the level for domain knowledge or experience of engineers, deep learning-based models have recently been studied. Since most previous studies aim to classify the single-type defect patterns, it is needed to consider the mixed-type defect patterns together. Also, they require a lot of labeled data to train the deep learning-based classification model. However, defects occur extremely rarely in actual manufacturing process. Therefore, the method securing the higher accuracy in a situation where enough labeled data are not given is needed. This paper proposes a deep convolutional generative adversarial network for wafer map synthesis (DCGAN-WS) which generates the mixed-type patterns by synthesizing the single-type pattern and adding the pixel-wise summation. To maintain the characteristics of the binary pixel of the wafer bin maps, a thresholding technique is added. MixedWM38 dataset is used for the experiments, and it was verified that the mixed-type patterns were synthesized well. It helps to construct more robust model for single-type pattern classification and to generate the mixed-type patterns that have not occurred before. In the future, it is expected that this model addresses the problem of the lack of labeled data for defect pattern classification models.**

Keywords— wafer bin maps, image synthesis, pattern classification, generative adversarial network

I. INTRODUCTION

In the semiconductor industry, there are several fine and complex production processes such as photolithography, etching, deposition, and cleaning to produce a chip. To increase productivity, the engineers manage yield and control factors that affect some defects. They check whether there are any process issues that cause defects during the manufacturing process for chips. And then, they inspect on each chip through the electrical die sorting (EDS) test, and divide each chip into "pass" or "fail". Wafer bin map is the result of the EDS test, and it is a map expressed as a binary pixel value according to the "pass" or "fail" of each chip. Defective chips identified as "fail" of each chip form a specific pattern on the wafer bin map. The EDS test results are expressed on the circular wafer map, and there may be various patterns depending on the position of the defective chips.

Fig. 1 shows normal pattern and several defect patterns such as *Center*, *Donut*, *Edge-Loc*, *Edge-Ring*, *Loc*, *Random*, *Scratch*, and *Near-full*. Each different patterns are caused by different factors. For example, *Center* pattern occurs when the solution is not uniformly polished on the wafer map in chemical mechanical polishing (CMP) process [1]. *Edge-Ring* pattern occurs due to a misalignment between layers in the process for accumulating layers on wafer maps [1]. *Scratch* pattern occurs due to the agglomerated particles and aging of the pad in CMP process [1]. Because the cause factors are different depending on the pattern types, it is important to accurately identify the defect patterns on the wafer bin map and to control the factors for reducing the defects.

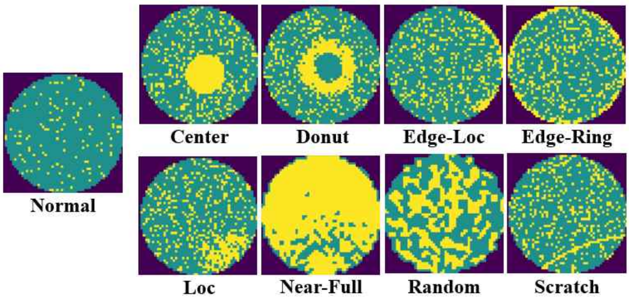

Fig. 1. Examples of the single-type defect patterns

To accurately obtain the consistent classification results regardless of the domain knowledge engineers when classifying defect patterns on wafer bin maps, many studies have been conducted to automatically classify defect patterns based on a model. There are studies that extract the features using transformation technique such as Wavelet transform and Radon transform and classify the patterns using machine learning-based models such as support vector machine (SVM), multilayer perceptron (MLP)), and radial basis function (RBF) [2, 3, 4].

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When using machine learning-based models for classifying the patterns, there is a difficulty in selecting a proper feature extraction method. To address this problem, deep learning-based models were proposed to perform both feature extraction and classification within a model. In particular, to recognize pattern by processing wafer bin maps as images, Convolutional neural network (CNN)-based model is used because it is known to be effective in image processing [5, 6, 7]. CNN classifies the defect patterns on the wafer bin map with high accuracy.

However, deep learning models such as CNN requires a number of labeled data for training to ensure high accuracy. In practice, it is hard to obtain a lots of labeled data in manufacturing process. Accordingly, unsupervised learning-based models such as density-based spatial clustering of applications with noise (DBSCAN) and self-organized map (SOM) are utilized because they do not require label information [8, 9]. This is useful in situations where labeled data are insufficient, but there is a disadvantage that performance is somewhat degraded compared to when labeled information is used together. Therefore, it is needed to study a model capable of securing high performance in a situation where a lots of labeled data are not given.

Also, there are not only single-type patterns but also mixed-type patterns in the actual manufacturing process. As shown in Fig. 2, the mixed-type patterns can be generated when two or more single-type patterns are mixed. If the mixed-type patterns are not recognized or the mixed-type patterns are incorrectly identified as a single-type pattern, all cause factors will not be controlled and defects continue to occur. Labeled data for the mixed-type patterns are more difficult to obtain because it occurs more rarely than single-type patterns. Mixed-type patterns can be generated through various combinations of single-type pattern, but data of all combinations may not be obtained. In this situation, if only the actually obtained mixed-type patterns are used only for training the models, it is hard to identify the mixed-type patterns when the other patterns appears.

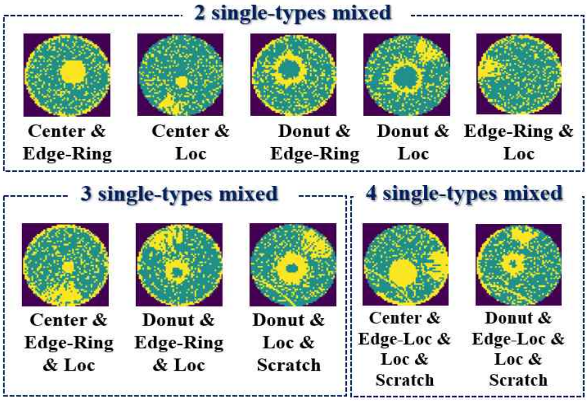

Fig. 2. Examples of the mixed-type defect patterns

Therefore, this paper proposes an image synthesis method that mixed-type patterns on wafer bin maps using only single-type patterns. Through this, a number of labeled samples that are difficult to obtain are generated. It helps to improve the classification performance of the model when a classification model is constructed using the generated data in the future. It also helps to make a robust model that can detect patterns that have not been mixed previously.

A deep convolutional generative adversarial network-based wafer map synthetic (DCGAN-WS) model is proposed in this paper. The proposed model consists several generators (G) for each single-type patterns for making variational data of single-type patterns and a discriminator (D) for classifying the real patterns and the generated patterns. The generated single-type patterns are used in a synthetic process for making mixed-type patterns. It makes to construct a more robust classification model for the single-type patterns and generates data for various types of the mixed-type patterns. The generated data from DCGAN-WS maintains the characteristics of the binary pixels on the wafer bin maps through the thresholding techniques. Then, the patterns are synthesized through a pixel-wise summation between the variational data considering the various combinations of the single-type patterns. Using the model, some variational data for single-type patterns and various cases for mixed-type patterns can be generated in a desired amount. The proposed method of this paper helps to get all information on single-type patterns and mixed-type patterns in the situation when the single-type patterns are given only. This addresses the problem of the lack of labeled data for defect pattern classification models.

Chapter 2 describes a proposed model, DCGAN-WS for synthesizing the mixed-type patterns. Chapter 3 shows the results of the synthesized maps. Finally, Chapter 4 describes the conclusion.

II. THE PRPOSED METHOD

This paper proposes an image synthesis method for wafer bin maps, called DCGAN-WS. DCGAN-WS has three steps, generating the variational data, thresholding for maintaining the characteristics of wafer bin maps and pattern synthesis using pixel-wise summation. The detailed description of each part are like the following.

A. Generating the Variational Data

The first step is to generate variational data for a single-type patterns using a deep convolutional generative adversarial network (DCGAN) model. DCGAN is a variants of the GAN containing deep convolutional layers [10]. It is divided into a generator part that generates new images and a discriminator part that distinguishes the generated images from the real images. The generator is comprised of transposed convolutional layers, batch norm layers, and ReLU activations. The input of the generator is a latent vector z from a standard normal distribution and the output is a RGB image. The discriminator is comprised of strided convolutional layers, batch norm layers, and Leaky ReLU activations. The input of discriminator is a input image and the output is the probability that the input is from the real data distribution.

Generators of are constructed as many as the number of the single-type patterns. For example, when there are six single-type patterns, the number of generator is six. Each generator makes variational data for each pattern by inserting the latent vector z as input. Since the generating process from a generator and the distinguishing process from a discriminator have adversarial learning, the generator can create variational images similar to the actual images that is difficult for the discriminator to distinguish. The overall framework of DCGAN is shown as Fig. 3.

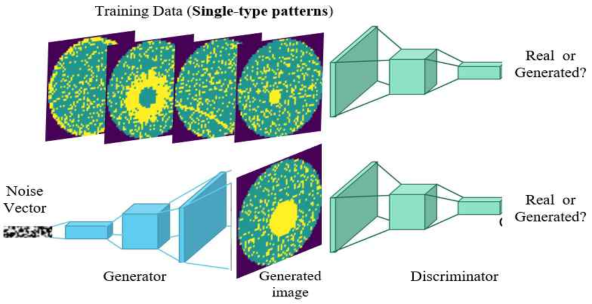

Fig. 3. The overall framework of DCGAN

B. *Thresholding Technique for Wafer Bin Map*

The output images of generators from the generator of DCGAN-WS have continuous pixel values on each pixel. However, the original wafer bin maps have only binary pixel values such as 0, 1, and 2 on each chip. Generally, 0 means empty part which the remaining edge part are filled with zero as the circular wafer maps are converted into a rectangular image. 1 means the "pass" or "good" chip in EDS test. 2 means the "fail" or "defective" chip in EDS test, and we have to focus on the defective part which forms a specific defect pattern. Therefore, it is needed to revise the characteristics of the pixel values same as the original wafer maps.

We can set a threshold empirically within the range from 0 to 1. The pixels of the generated images consist of continuous values from 0 to 1. By setting two thresholds which one is for dividing 0 (empty part) and 1 (pass chip) and the other is for dividing 1 (pass chip) and 2 (fail chip). When the thresholds are set, the binary pixel values are assigned to each pixel, as shown in Fig. 4. After thresholding, the defect patterns can be clarified on wafer bin maps. Although the thresholds are defined empirically in this paper, the further studies for appropriate thresholds are necessary because the shape and size of defect patterns can be changed according to the thresholding.

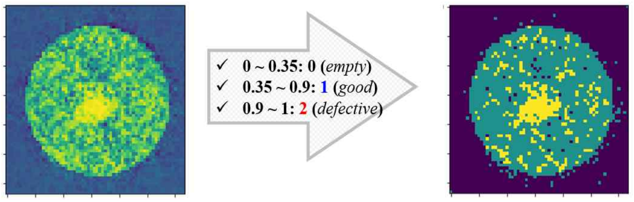

Fig. 4. Result for the thresholding technique

C. *Pattern Synthesis using Pixel-wise Summation*

After passing the DCGAN and thresholding, there are many variational images for each single-type pattern. The mixed-type patterns are formed by the combinations of multiple single-type patterns. By combining the generated single-type patterns, the mixed-type patterns can be generated as much as the desired amounts.

To synthesize the single-type patterns, the pixel-wise summation is used on multiple single-type patterns. Pixel-wise summation is to add the pixel values at the same location on wafer bin maps as shown in Fig. 5. When several maps are sampled randomly from the generated maps of single-type patterns, the added values are calculated to the same location on wafer bin maps from the samples. When two single-type patterns are sampled, the mixed-type pattern which is combined by two single-type patterns can be generated. Also, when three single-type patterns are sampled, the mixed-type pattern which is combined by three single-type patterns can be generated. And then, the threshold in Section 2.B is repeated to represent the pixel values as binary type.

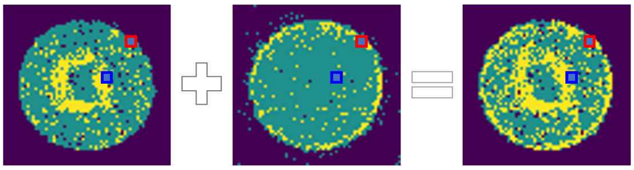

Fig. 5. The result for the pixel-wise summation for mixed-type synthesis

This procedure utilizes the generated variational data from the single-type patterns. Therefore, it helps to make robust model for single-type patterns and synthesize the various mixed-type patterns although it is same defect patterns.

III. EXPERIMENTALS

A. *Data Description*

The dataset for experiments is *MixedWM38* dataset which are used in [11]. The data contain a *Normal* pattern (no defects), 8 single-type defect patterns such as *Center*, *Donut*, *Edge-Loc*, *Edge-Ring*, *Loc*, *Near-Full*, *Random*, *Scratch*, and mixed-type defect patterns which are combined by two or three or four single-type patterns. The number of types for the mixed-type pattern combined by two single-type patterns is 13 and the number of types for the mixed-type pattern combined by three single-type patterns is 11, and the number of types for the mixed-type patterns combined by four single-type patterns is 2. The number of single-type patterns are 1,000 images on each pattern. Because this paper focuses on the defect patters, especially the mixed-type patterns, the target defect patterns are 6 patterns such as *Center*, *Donut*, *Edge-Loc*, *Edge-Ring*, *Loc*, *Scratch*.

B. *Experimental Results*

The proposed model, DCGAN-WS, is constructed by three steps, generating the variational data with DCGAN, thresholding for maintaining the characteristics of wafer bin maps, and generating the mixed-type patterns by synthesizing multiple single-type patterns.

In first step, the architecture of DCGAN is same as [10]. When DCGAN is trained, the setting parameters are set like this. The epoch is 20, batch size is 100, learning rate is 0.0001, and the optimizer is Adam. In this step, the generator of DCGAN-WS generates each single-type pattern. The generated maps are shown in Fig. 6. The most generated patterns are similar to the real wafer bin maps. However, *Edge-Loc* and *Scratch* is relatively not similar to the real wafer bin maps. Although actual

Edge-Loc has the half of the ring pattern on the edge of the wafer map, the results for Edge-Loc contains some circular patterns, not ring shape. Also, the Scratch pattern is a linear pattern located randomly on the map. However, the result for the *Scratch* pattern shows the patterns like *Random*. Therefore, further studies for *Edge-Loc* and *Scratch* is needed to improve the performance of generating the single-type patterns, because it affects the quality of the synthesized mixed-type pattern.

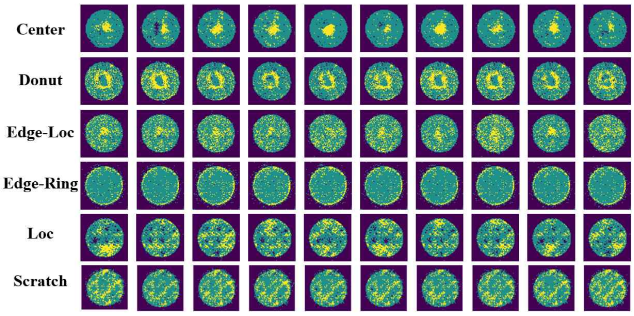

Fig. 6 The results for generating the variational single-type patterns

Using the results in Fig. 5, the variational data for each single-type pattern are utilized to synthesize the mixed-type patterns. By adding the pixel-wise summation to the randomly sampled variational data, several mixed-type patterns can be generated. After the summation, the thresholding technique is repeated to represent the characteristics of wafer bin maps. In this paper, the mixed-type patterns are defined as the synthesized results of two single-type patterns only. Fig. 7 shows the synthesized mixed-type patterns by combining the single-type patterns. Edge-Loc and Scratch which are not similar to the actual pattern in first step cannot still be mixed well. Therefore, to improve the quality of generated variational data for single-type patterns and the quality of the synthesized mixed-type patterns, it is important to improve the method for generating poor patterns for the single-type.

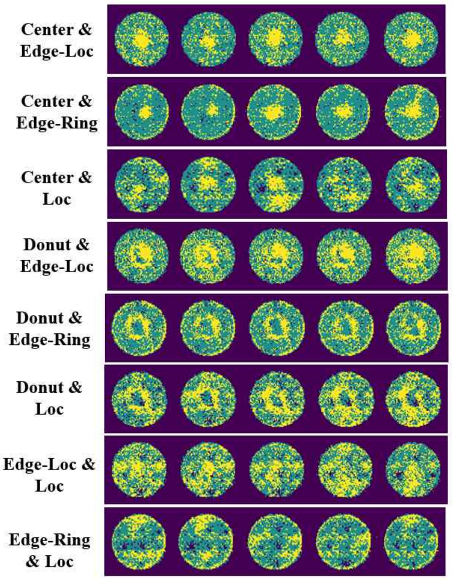

Fig. 7. The synthesized results for the mixed-type patterns

IV. CONCLUSION

The studies for automatic defect classification model have been conducted because it is important to check the defect patterns on the wafer bin maps and control the cause factors for yield improvement in semiconductor manufacturing. To address the limitations of the previous deep learning-based model, it is needed to consider the mixed-type defect patterns and secure the higher accuracy in situation where enough labeled data are not given. This paper proposed a deep convolutional generative adversarial network for wafer map synthesis (DCGAN-WS) which generates the mixed-type patterns by synthesizing the single-type pattern. First, DCGAN is applied to generate the variational data of the single-type patterns. The generated maps are sampled randomly and they are added using the pixel-wise summation. To maintain the characteristics of the binary pixel of the wafer bin maps, the thresholding technique is utilized. Using the MixedWM38 dataset as the experimental data, it was verified that the mixed-type patterns were synthesized well. However, some patterns such as *Edge-Loc* and *Scratch* are needed to study more for generating the maps similar to the real patterns. The proposed method helps to construct more robust model for single-type pattern classification although the number of data is lack or there is a class imbalance. Also, It helps to generate the mixed-type patterns that have not occurred before. In the future, it is expected that this model addresses the problem of the lack of labeled data for defect pattern classification models.

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