Modified Phase-Shift PWM for Common-Mode Voltage Reduction in PMSM Drives Fed by Five-Level HANPC Inverter

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***Abstract*--This study proposes a modified phase-shift pulse width modulation (PS-PWM) technique for reducing common-mode voltage (CMV) in five-level hybrid active neutral-point-clamped (HANPC) inverters fed permanent magnet synchronous motor (PMSM). The proposed method is based on restricting the injection of a zero-sequence voltage at sections where CMV has its peak values. A comparison between the proposed modified PS-PWM and the conventional PS-PWM was conducted using simulation results obtained from PSIM software. The results indicated that the proposed modified PS-PWM technique led to a significant reduction of 50% in CMV compared to the conventional PS-PWM method. This study highlights the effectiveness of the proposed modified PS-PWM technique in reducing the CMV in five-level HANPC inverters fed PMSMs through the strategic injection of a zero-sequence voltage.**

***Index Terms*—Common-mode voltage (CMV) reduction, five-level hybrid active neutral-point-clamped (HANPC) inverter, permanent magnet synchronous motors, phase-shift pulse-width-modulation (PWM).**

I. Introduction

The use of permanent magnet synchronous motors (PMSMs) has become widespread in various industrial medium voltage applications due to their high torque, efficiency, and power density [1]–[3]. Despite these advantages, PMSM drives face a major challenge in the form of common-mode voltage (CMV). This CMV can lead to leakage currents and voltage stresses in the drive system, ultimately reducing the lifetime of the PMSM [4].

To mitigate the effects of CMV, various approaches have been proposed, including multilevel hybrid active neutral-point-clamped (HANPC) inverters. In case of three-level HANPC inverter, the reduction or elimination techniques have been presented in [5]–[7]. However, these approaches suffer from high output current distortion and limitation in applicable modulation index operation. For example, the authors in [6] introduced an effective CMV elimination method by utilizing only medium and zero voltage vectors as they produce zero CMV. Although an elimination of CMV is achieved, the modulation requires complex dwelling time calculation and is not applicable in modulation range > 0.86. Thus it is not recommend in motor drives where high-speed operation is essential in most industrial applications.

For five-level HANPC inverter, it possess several advantages over other multilevel inverter topologies, such as a smaller number of active switching devices (S_{x1}–S_{x8}) and flying capacitors (C_{fx}), where x represents the three-phases a, b, and c, as shown in the circuit topology in Fig. 1 [8]–[12]. An approach utilizing fifty-five voltage vectors, has been introduced for reducing the CMV to $V_{DC}/12$ in five-level inverters [13]. However, the balance of the dc-link capacitor voltage, requiring four controllable dc sources, has not been investigated in this scheme. In the case of three-phase five-level cascaded H-bridge inverters, the CMV value can be decreased to $V_{DC}/12$ without dc capacitor voltage control, but it may not be applicable to five-level HANPC inverters [14].

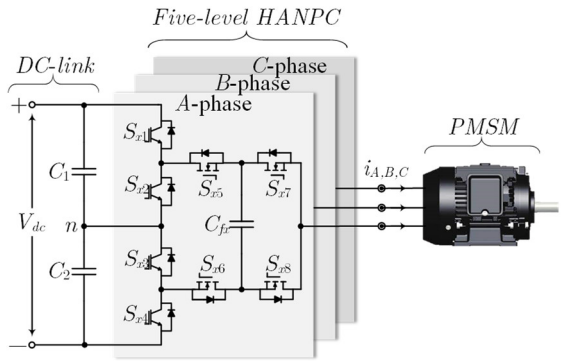


Fig. 1. Circuit topology of a three-phase five-level HANPC inverter feeding a three-phase load.

Another approach is presented in [15], which utilizes 55 voltage vector among the total 125 voltage vectors used for controlling the five-level HANPC inverter. Although, a noticeable suppression is achieved, this method depends on fine tuning and complex calculation of duty cycles of each voltage vector in order to balance the dc-link capacitors voltages as well as flying capacitor voltages. An elimination of CMV is presented in [16] by utilizing only 19 voltage vectors, which produce zero CMV. This technique requires additional adjustment and complex arrangement of redundant switching states of voltage vectors responsible for balancing dc-link capacitors voltages in addition to voltages across flying capacitors. Furthermore, it suffers from applicable maximum modulation index to 0.86. Thus, it is not desirable for applications requiring high-speed operation.

In order to address the above mentioned limitations, this study presents a modified phase-shift pulse-width modulation (PS-PWM) technique for reducing the CMV in five-level HANPC inverters fed PMSMs. The proposed technique restricts the injection of a zero-sequence voltage

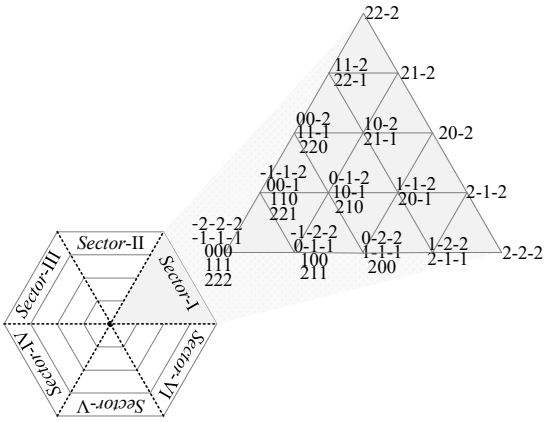


Fig. 2. Space representation of voltage vectors utilized by a five-level HANPC inverter.

at sections exhibiting the highest absolute values of CMV. This leads to a substantial minimization on the CMV in addition to balancing the dc-link of the five-level HANPC inverter. Simulation results obtained through the use of PSIM software demonstrate a significant reduction of 50% in the CMV compared to the conventional PS-PWM method. This proposed technique offers an innovative solution for improving the performance of PMSM drive and mitigating the impact of CMV on the drive system.

II. System Modelling

A. Five-Level HANPC Inverter

As explained briefly in the previous section that the five-level HANPC inverter has been built in accordance with maintaining excellent performance to effective cost [10]. This topology has the ability to produce a five-level output voltage due to an effective modulation control which is required to balance the voltages across the dc-link capacitors (i.e., C_1 and C_2) as well as the voltages across C_{fx} in the three phases of the five-level HANPC inverter. This could be done by using a proper modulation scheme that is able to balance these voltages such as PS-PWM, as shown from space diagram of voltage vectors in Fig. 2 and their corresponding voltage states shown in Table I.

To simplify the control and balance the switches losses in this topology, a hybrid modulation scheme is utilized. It is worthy to mention that there two types of active switching devices used in this inverter. Si IGBT switching devices are known for their capability to block high voltage however they suffer in high frequency range. Therefore, they are used at fundamental frequency in switching devices (S_{x1}–S_{x4}). In order to enhance the system performance and produce less distorted output waveforms. A high frequency PWM modulation is desirable to control the switching devices (S_{x5}–S_{x8}). As result, SiC MOSFET can be a good candidate for high frequency operation considering their ability to maintain acceptable thermal distribution. In this scenario, a filter size is much minimized, which reduce the volume and cost of the system.

B. Current Control of PMSM

A three-phase PMSM is considered in this study, which is fed by a five-level HANPC inverter, as shown in Fig. 1. It is important to analyze the model of PMSM in order to simplify its control as desired. Therefore, voltage equations for a PMSM in the *d-q* reference frame of the rotor using field-oriented control are described as in (1),

$$\begin{cases} v_d = k_{pd} I_{derr} + k_i I_{dierr} T_s - \omega_e L_q I_q \\ v_q = k_{pq} I_{qerr} + k_i I_{qierr} T_s + \omega_e L_d I_d + \omega_e \ \phi_f \end{cases}. \quad (1)$$

In the *d-q* rotating reference frame, v_d and v_q represent the voltage components, while I_{derr}, I_{qerr}, I_{dierr}, I_{qierr}, I_d, and I_q denote the error, integration error, and estimated current components. The inductances are L_d and L_q, and the electrical rotor speed is ω_e. Additionally, φ_f represents the flux linkage established by the rotor. The proportional and integral gains, k_p and k_i, respectively, are calculated as in (2),

$$\begin{cases} k_{pd} = L_d \omega_{cc} \\ k_{pq} = L_q \omega_{cc} \\ k_i = R_s \omega_{cc} \end{cases}. \quad (2)$$

The current control bandwidth, denoted as ω_{cc}, can be chosen as 1/10th of the switching frequency (f_{sw}) [17]. The stator resistance per phase is represented by R_s. To convert the *d-q* voltages to *α-β* voltages in the stationary reference frame, the inverse Park's transformation can be used as provided in (3),

$$\begin{cases} v_\alpha = v_d \cos(\theta_r) - v_q \sin(\theta_r) \\ v_\beta = v_d \cos(\theta_r) + v_q \sin(\theta_r) \end{cases}. \quad (3)$$

Then *α-β* voltages can be converted into three-phase reference voltages (v_{as}^*, v_{bs}^*, and v_{cs}^*) as expressed in (4),

TABLE I
Voltage states of five-level HANPC inverter

Voltage states	S_{x1} S_{x3} $\bar{S}_{x2}$ $\bar{S}_{x4}$	S_{x5} $\bar{S}_{x6}$	S_{x7} $\bar{S}_{x8}$	v_{xn}	I_n	I_{cfx}
V_1	1	1	1	$V_{dc}/2$	0	0
V_2	1	1	0	$V_{dc}/4$	$-I_x$	0
V_3	1	0	1	$V_{dc}/4$	I_x	I_x
V_4	1	0	0	0	0	I_x
V_5	0	1	1	0	0	I_x
V_6	0	1	0	$-V_{dc}/4$	$-I_x$	I_x
V_7	0	0	1	$-V_{dc}/4$	I_x	0
V_8	0	0	0	$-V_{dc}/2$	0	0

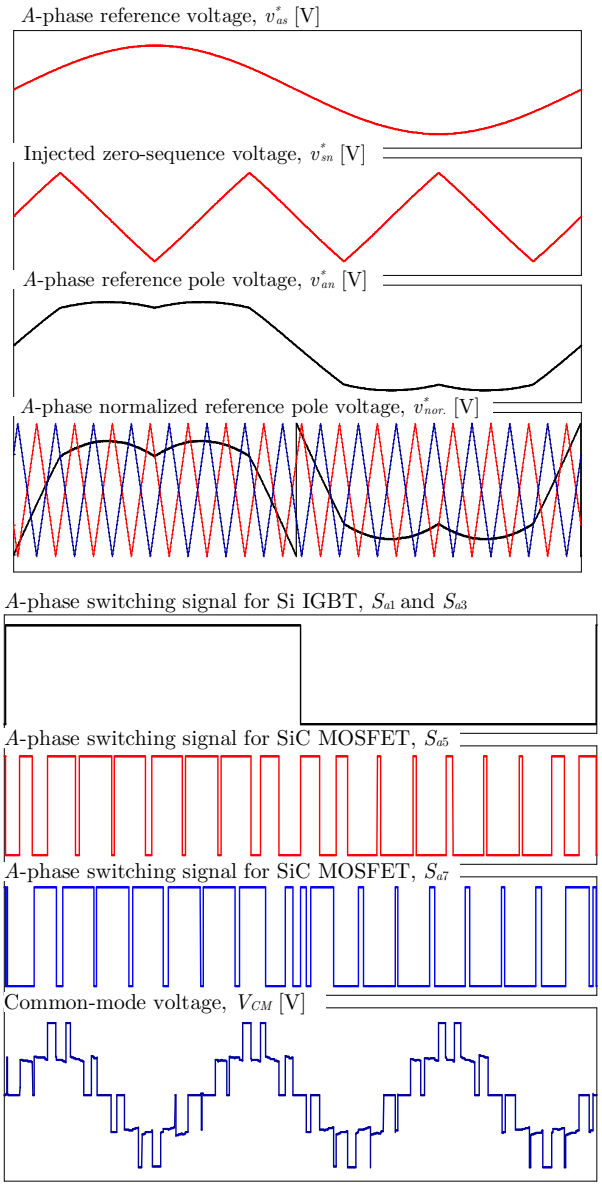


Fig. 3. Operational principle of conventional PS-PWM with injection of zero-sequence voltage v^*_{sn}. The CMV is switching in five different levels as $-V_{dc}/6 \rightarrow -V_{dc}/12 \rightarrow 0 \rightarrow V_{dc}/12 \rightarrow V_{dc}/6$.

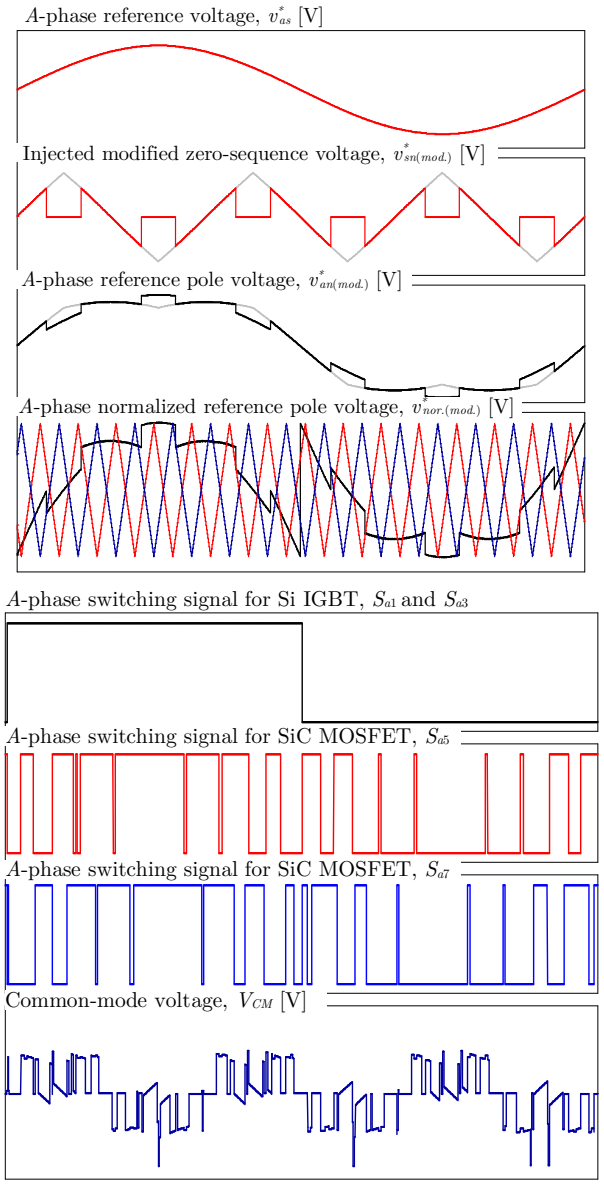


Fig. 4. Operational principle of modified PS-PWM with injection of a new zero-sequence voltage $v^*_{sn(mod.)}$. The suppressed CMV is switching in three different levels as $-V_{dc}/12 \rightarrow 0 \rightarrow V_{dc}/12$.

$$\begin{cases} v^*_{as} = v_\alpha \\ v^*_{bs} = -\dfrac{1}{2}v_\alpha + \dfrac{\sqrt{3}}{2}v_\beta \\ v^*_{cs} = -\dfrac{1}{2}v_\alpha - \dfrac{\sqrt{3}}{2}v_\beta \end{cases}. \tag{4}$$

By using the three-phase reference voltages in (4), the switching signals sent to S_{x1}–S_{x8} are generated using a proper modulation scheme.

C. Conventional PS-PWM Switching Scheme

It is worthy to note that PS-PWM can be considered one of the best candidates used to control the five-level HANPC inverter for its robust and natural ability to balance the voltages across C_{fx} as well as maintain a balanced neutral-point. In addition, the switching losses are equally distributed among the switching devices [10]. Fig. 3 shows the operational principle of the conventional PS-PWM and its effect to produce a large CMV, which is switching as $-V_{dc}/6 \rightarrow -V_{dc}/12 \rightarrow 0 \rightarrow V_{dc}/12 \rightarrow V_{dc}/6$.

To extend the modulation index by 15.5% [17] for reduced the distortion of the output voltage waveforms, a zero-sequence voltage (v^*_{sn}) needs to be injected into the system to generate the reference pole voltage (v^*_{an}) as expressed in (5),

$$v^*_{an} = v^*_{as} + v^*_{sn}, \tag{5}$$

where v_{sn}^{*} is obtained by considering the maximum and minimum values of the three-phase, as shown in (6),

$$v_{sn}^{*} = -\left(\frac{\max\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\} + \min\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\}}{2}\right). \tag{6}$$

Then v_{an}^{*} is normalized ($v_{an,nor.}^{*}$) and compared with the PWM carriers to generate the switching signals for the five-level HANPC inverter. The normalized $v_{an,nor.}^{*}$ can be expressed as in (7),

$$v_{an,nor.}^{*} = \begin{cases} \left(\frac{2 \times v_{an}^{*}}{V_{dc}}\right), & + \text{half cycle} \\ 1 + \left(\frac{2 \times v_{an}^{*}}{V_{dc}}\right), & - \text{half cycle} \end{cases}. \tag{7}$$

The switching signal for Si IGBT switching devices are generated and switching at the fundamental frequency without the need for the PWM carriers, as expressed in (8),

$$S_{x1} \text{ and } S_{x3} = \begin{cases} \text{ON}, & + \text{half cycle} \\ \text{OFF}, & - \text{half cycle} \end{cases}. \tag{8}$$

However, the switching signals generated for SiC MOSFET switching devices are dependent on PWM interleaved carriers as shown in Fig. 3 and given in (9),

$$S_{x5} = \begin{cases} \text{ON}, & v_{an,nor.}^{*} \geq Carrier1 \\ \text{OFF}, & v_{an,nor.}^{*} < Carrier1 \end{cases}, \quad S_{x7} = \begin{cases} \text{ON}, & v_{an,nor.}^{*} \geq Carrier2 \\ \text{OFF}, & v_{an,nor.}^{*} < Carrier2 \end{cases}. \tag{9}$$

Although the conventional PS-PWM scheme has a very simple switching scheme that can generate the desired five-level output pole voltage, v_{an}^{*} with balanced neutral-point and voltages across C_{fx}, it suffers from producing high CMV with peak value of $V_{dc}/6$ which can reduce the reliability of the drive system.

TABLE II
PMSM PARAMETERS

Parameter	Value [unit]
Rated power	5 [kW]
Rated current	17.23 [A]
Rated torque	27.3 [Nm]
Rated speed	1750 [r/min]
Stator resistance	0.158 [Ω]
d-axis inductance	0.00729 [H]
q-axis inductance	0.00725 [H]
Moment of inertia	0.00666 [kg·m^2]
Permanent magnet flux	0.264 [Wb]
Number of poles	8

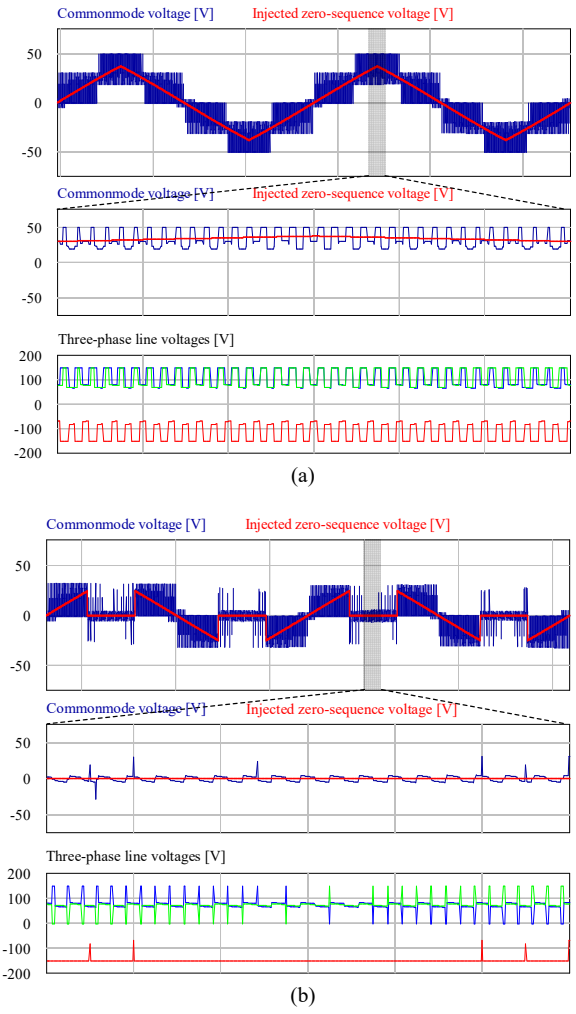
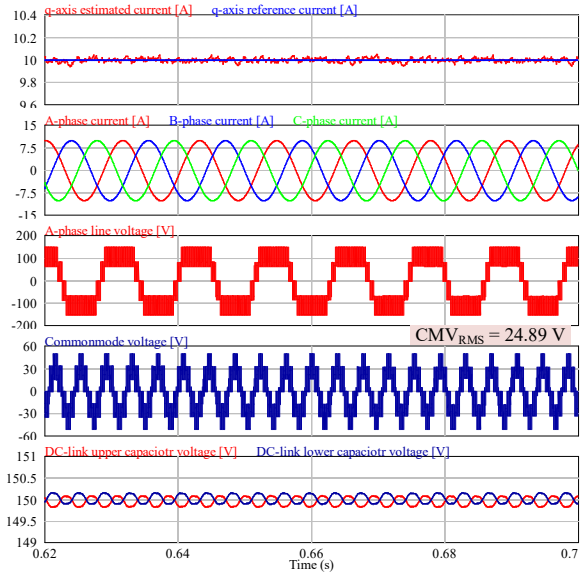
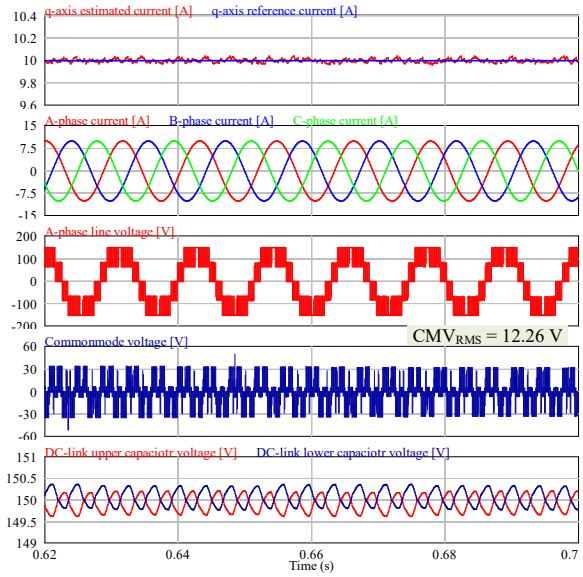


Fig. 5. Effect of injected zero-sequence voltage on CMV. (a) Conventional PS-PWM. (b) Modified PS-PWM.

$$v_{sn(\text{mod.})}^{*} = \begin{cases} 0, & \begin{cases} \left(\max\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\} / 2 \geq v_{sn}^{*} \geq \max\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\} / 4\right) \\ \left(\min\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\} / 4 \geq v_{sn}^{*} \geq \min\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\} / 2\right) \end{cases} \\ -\left(\frac{\max\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\} + \min\{v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\}}{2}\right), & otherwise \end{cases}. \tag{10}$$

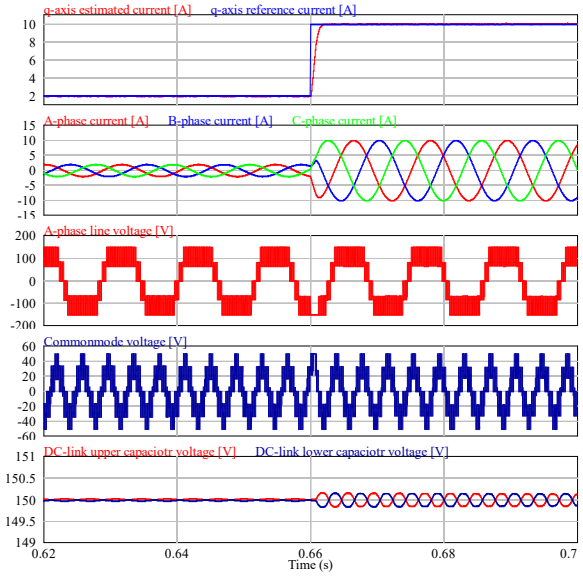


(a)

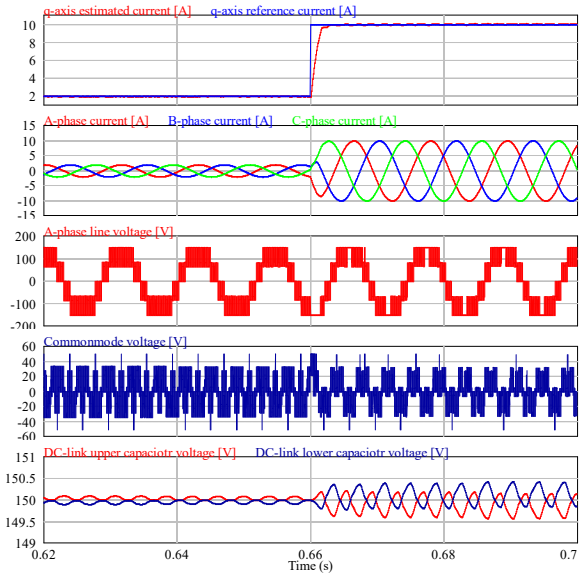


(b)

Fig. 6. Performance evaluation of PMSM drive system at 1300 r/min with a reference current of 10 A. (a) Conventional PS-PWM. (b) Modified PS-PWM.



(a)



(b)

Fig. 7. Performance evaluation of PMSM drive system at 1300 r/min with a step change in reference current from 2 to 10 A. (a) Conventional PS-PWM. (b) Modified PS-PWM.

D. Modified PS-PWM Switching Scheme

To mitigate the effects of CMV, a modified PS-PWM is proposed for five-level HANPC inverter fed PMSM. It is worth mentioning that the proposed modified PS-PWM does not require any complex dwelling time calculation for each selected voltage vector in order to reduce the CMV as presented in [10]. Alternatively, the proposed modified PS-PWM switching scheme maintains the simplicity and the natural ability of the conventional PS-PWM in balancing the five-level HANPC inverter.

The proposed switching scheme restricts the utilization of injected zero-sequence voltage at sections where CMV has its peak values (i.e., CMV = $V_{DC}/6$). The modified injected zero-sequence voltage ($v^*_{sn(mod.)}$) is calculated as in (10), as shown in the bottom of the previous page. As a result, v^*_{an} can be expressed in terms of $v^*_{sn(mod.)}$ as in (11),

$$v^*_{an} = v^*_{as} + v^*_{sn(\mathrm{mod.})}. \tag{11}$$

Finally, the CMV can be reduced by 50% by eliminating half of its amplitude. Therefore, the CMV is switching between $-V_{dc}/12$, 0, and $V_{dc}/12$ by using the proposed modified PS-PWM as shown in Fig. 4. The CMV can be calculated by (12) as,

$$CMV = \left(v_{an} + v_{bn} + v_{cn}\right) / 3. \tag{12}$$

III. Simulation Results and Discussion

The effectiveness of the proposed modified PS-PWM switching scheme against the conventional PS-PWM is demonstrated by comprehensive simulation results as shown in Figs. 5, 6, and 7. The simulation has been done by using PSIM software where the PWM carrier f_{sw} is set as 30 kHz to ensure better THD characteristics of output voltages and reduce filter size [10]. Table II illustrates the parameters of the PMSM used in this study. The DC-link is set to 300 V. Therefore, the base speed of the PMSM is 1300 r/min.

It can be shown from Fig. 5 (a) that the conventional PS-PWM produces a CMV with peak value of $V_{DC}/6$. It is noticeable that v_{sn}^{*} has the same frequency as the CMV and its peak values are at the same sections where the CMV values are switching between $V_{dc}/6$ and $V_{dc}/12$ or $-V_{dc}/12$ and $-V_{dc}/6$. Conversely, the modified PS-PWM switching scheme eliminates the peak values of the CMV by modifying the injected zero-sequence voltage at those sections, as shown in Fig. 5 (b). Therefore, a substantial reduction is achieved, resulting in a CMV with a peak value of $V_{dc}/12$.

In addition, the proposed and conventional PS-PWM techniques are evaluated at 1300 r/min with a reference current of 10 A, as shown in Fig. 6 and with a step change from 2 to 10 A, as shown in Fig. 7. The results indicate that the modified PS-PWM suppresses the CMV to a 50% of its RMS value. Moreover, the dc-link voltages are balanced, which results in a stable operation of the PMSM with a noticeable reduction on the CMV and without the need for complex tuning of voltage vector adjustments.

IV. Conclusions

In conclusion, this study has proposed a modified PS-PWM technique for minimizing the CMV in five-level HANPC inverter fed PMSM. The proposed method is based on restricting the injection of the zero-sequence voltage at the sections where CMV has its peak values of $|V_{dc}/6|$. It is worth mentioning that the proposed technique maintains the merits of the conventional PS-PWM in naturally balancing the capacitors voltages without the need for complex voltage vectors adjustments. Simulation results indicate that the proposed modified PS-PWM technique results in a substantial reduction of 50% in the CMV compared to the conventional PS-PWM method. In addition, the system is kept stable and balanced during the implementation of the proposed PS-PWM.

Acknowledgment

This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry & Energy (MOTIE) of the Republic of Korea (No. 20225000000110).

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